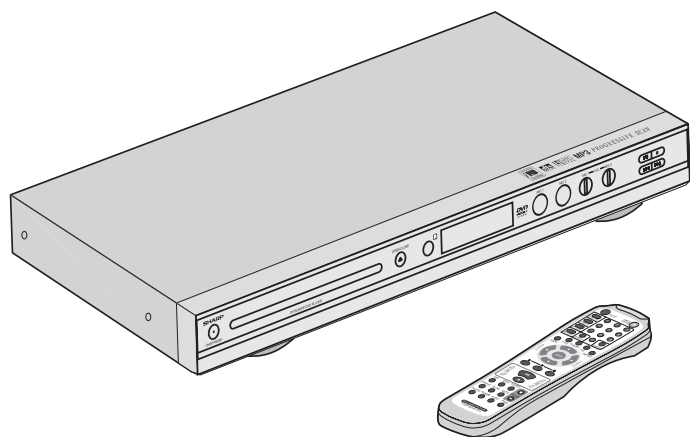


SHARP SERVICE MANUAL

No.S9504DVSL800W



DVD PLAYER MODEL DV-SL800W

- In the interests of user-safety (Required by safety regulations in some countries) the set should be restored to its original condition and only parts identical to those specified be used.



CONTENTS

	Page
SAFETY PRECAUTION FOR SERVICE MANUAL	2
AC POWER SUPPLY CORD	2
SPECIFICATIONS.....	3
LASER BEAM SAFETY PRECAUTIONS	4
STANDARD NOTES FOR SERVICING	5
OPERATING CONTROLS AND FUNCTIONS.....	8
BLOCK DIAGRAMS	10
SCHEMATIC DIAGRAMS	12
IC'S PIN VOLTAGE CHART.....	26
WAVEFORMS	29
OVERALL WIRING CONNECTION	32
WIRING DIAGRAM	34
NOTES ON SCHEMATIC DIAGRAM/TYPES OF TRANSISTOR AND LED	44
TROUBLESHOOTING	45
IC PIN FUNCTION DESCRIPTIONS	46
FL DISPLAY	74
PARTS GUIDE/EXPLODED VIEW	

Parts marked with "▲" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

This document has been published to be used for after sales service only.
The contents are subject to change without notice.

SAFETY PRECAUTION FOR SERVICE MANUAL

● This product is classified as a CLASS 1 LASER PRODUCT.

● **WARNINGS:**

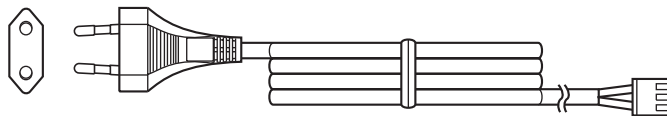
The AEL (Accessible Emission Level) of Laser Power Output for this model is specified to be lower than Class 1 Requirements. However, the following precautions must be observed during servicing to protect your eyes against exposure to the Laser beam.

- (1) When the cabinet has been removed, the power is turned on without a compact disc, and the Pickup is on a position outer than the lead-in position, the Laser will light for several seconds to detect a disc. Do not look into the Pickup Lens.
- (2) The Laser Power Output of the Pickup inside the unit and replacement service parts have already been adjusted prior to shipping.
- (3) No adjustment to the Laser Power should be attempted when replacing or servicing the Pickup.
- (4) Under no circumstances look directly into the Pickup Lens at any time.
- (5) CAUTION - Use of controls or adjustments, or performance of procedures other than those specified herein may result in hazardous radiation exposure.

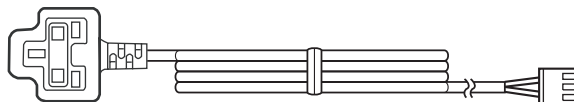
AC POWER SUPPLY CORD



92LCCP01000430



92LVPE00327911



92LVPE41A25310

SPECIFICATIONS

As part of our policy of continuous improvement, SHARP reserves the right to make design and specification changes for product improvement without prior notice. The performance specification figures indicated are nominal values of production units. There may be some deviations from these values in individual units.

● General

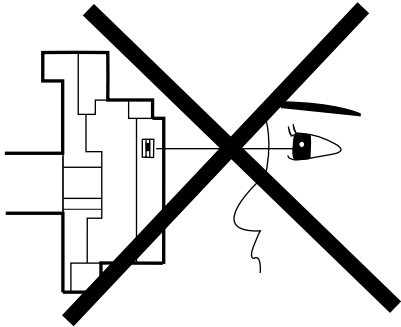
Power source	AC 110~240 V, 50/60 Hz
Power consumption	Power on:12W
Dimensions	Width: 430 mm (16-15/16") Height: 37 mm (1-1/2") Depth: 200 mm (7-7/8")
Weight	1.70 kg (3.75 lbs.)
Audio input terminals	MIC x 2 (ø6.3)
Audio output terminals	Analogue output (OUT): RCA type x 1 pair (L/R)
Video output terminals	S-video output: S-terminal x 1, Component video output: (Y, PB, PR) Video output: RCA type x 1
Digital output terminals	COAXIAL

● DVD player

Signal system	PAL/NTSC colour	
Supported disc types	DVD (with the same region number on the back of the unit), SVCD, VCD, audio CD, CD-R, CD-RW, MP3, JPEG	
Video signal	Horizontal resolution: 500 lines S/N ratio: 70 dB	
Audio signal	Frequency characteristics	Linear PCM DVD: 20 Hz to 20 kHz (sampling rate: 48 kHz) 20 Hz to 20 kHz (sampling rate: 96 kHz) CD: 20 Hz to 20 kHz
	S/N ratio	CD: 94 dB (1 kHz)
	Dynamic range	Linear PCM DVD: 95 dB CD: 94 dB
	Total harmonic distortion ratio	0.01 % maximum

LASER BEAM SAFETY PRECAUTIONS

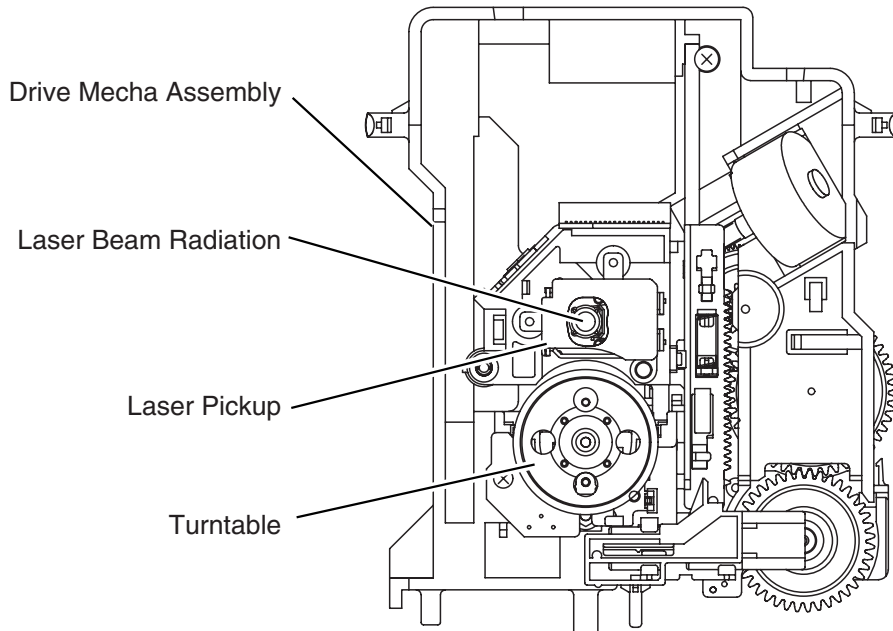
This DVD player uses a pickup that emits a laser beam.



Do not look directly at the laser beam coming from the pickup or allow it to strike against your skin.

The laser beam is emitted from the location shown in the figure. When checking the laser diode, be sure to keep your eyes at least 30cm away from the pickup lens when the diode is turned on. Do not look directly at the laser beam.

Caution: Use of controls and adjustments, or doing procedures other than those specified herein, may result in hazardous radiation exposure.



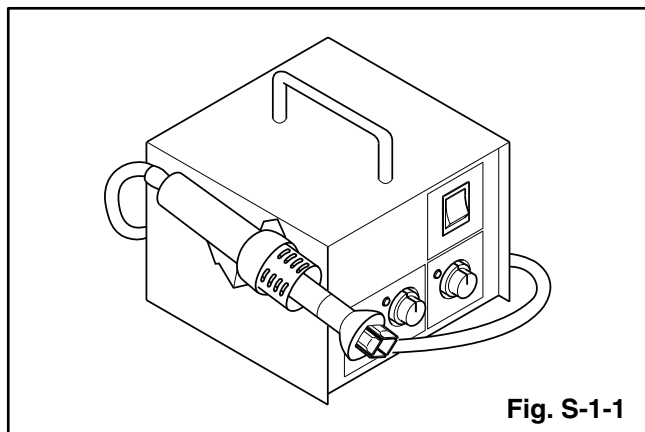
STANDARD NOTES FOR SERVICING

How to Remove / Install Flat Pack-IC

1. Removal

With Hot-Air Flat Pack-IC Desoldering Machine:

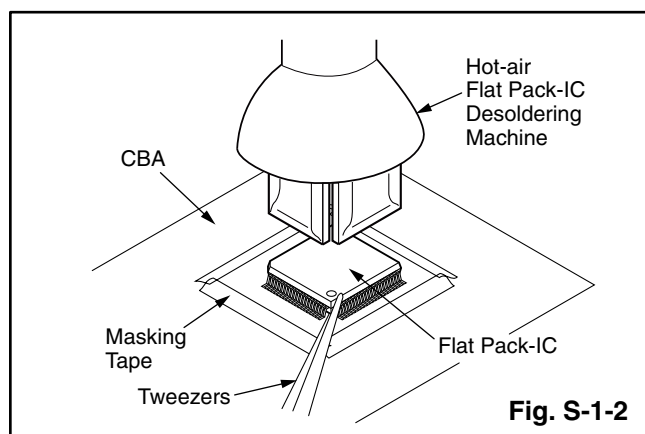
- (1) Prepare the hot-air flat pack-IC desoldering machine, then apply hot air to the Flat Pack-IC (about 5 to 6 seconds). (Fig. S-1-1)



- (2) Remove the flat pack-IC with tweezers while applying the hot air.
- (3) Bottom of the flat pack-IC is fixed with glue to the CBA; when removing entire flat pack-IC, first apply soldering iron to centre of the flat pack-IC and heat up. Then remove (glue will be melted). (Fig. S-1-6)
- (4) Release the flat pack-IC from the CBA using tweezers. (Fig. S-1-6)

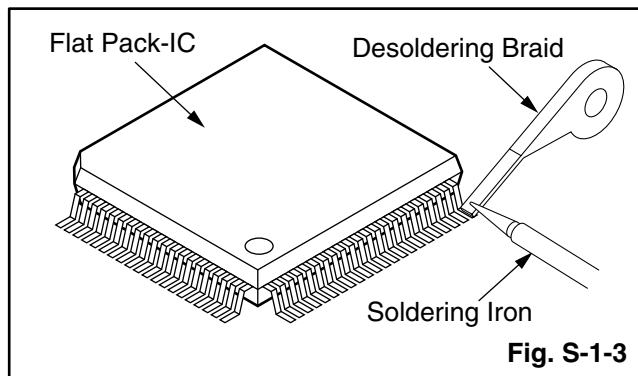
Caution:

1. Do not supply hot air to the chip parts around the flat pack-IC for over 6 seconds because damage to the chip parts may occur. Put masking tape around the flat pack-IC to protect other parts from damage. (Fig. S-1-2)
2. The flat pack-IC on the CBA is affixed with glue, so be careful not to break or damage the foil of each pin or the solder lands under the IC when removing it.

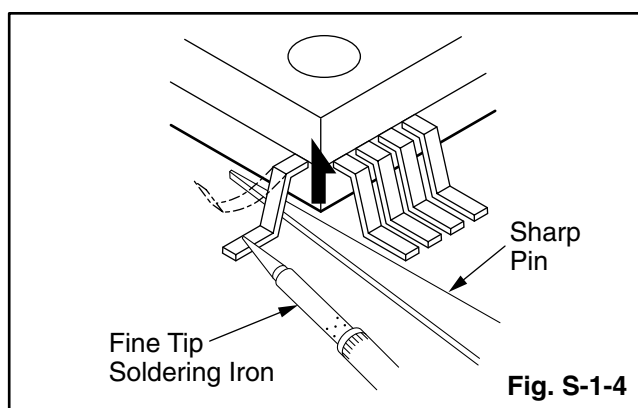


With Soldering Iron:

- (1) Using desoldering braid, remove the solder from all pins of the flat pack-IC. When you use solder flux which is applied to all pins of the flat pack-IC, you can remove it easily. (Fig. S-1-3)



- (2) Lift each lead of the flat pack-IC upward one by one, using a sharp pin or wire to which solder will not adhere (iron wire). When heating the pins, use a fine tip soldering iron or a hot air desoldering machine. (Fig. S-1-4)



- (3) Bottom of the flat pack-IC is fixed with glue to the CBA; when removing entire flat pack-IC, first apply soldering iron to centre of the flat pack-IC and heat up. Then remove (glue will be melted). (Fig. S-1-6)
- (4) Release the flat pack-IC from the CBA using tweezers. (Fig. S-1-6)

With Iron Wire:

- (1) Using desoldering braid, remove the solder from all pins of the flat pack-IC. When you use solder flux which is applied to all pins of the flat pack-IC, you can remove it easily. (Fig. S-1-3)
- (2) Affix the wire to a workbench or solid mounting point, as shown in Fig. S-1-5.
- (3) While heating the pins using a fine tip soldering iron or hot air blower, pull up the wire as the solder melts so as to lift the IC leads from the CBA contact pads as shown in Fig. S-1-5.

- (4) Bottom of the flat pack-IC is fixed with glue to the CBA; when removing entire flat pack-IC, first apply soldering iron to centre of the flat pack-IC and heat up. Then remove (glue will be melted). (Fig. S-1-6)
- (5) Release the flat pack-IC from the CBA using tweezers. (Fig. S-1-6)

Note:

When using a soldering iron, care must be taken to ensure that the flat pack-IC is not being held by glue. When the flat pack-IC is removed from the CBA, handle it gently because it may be damaged if force is applied.

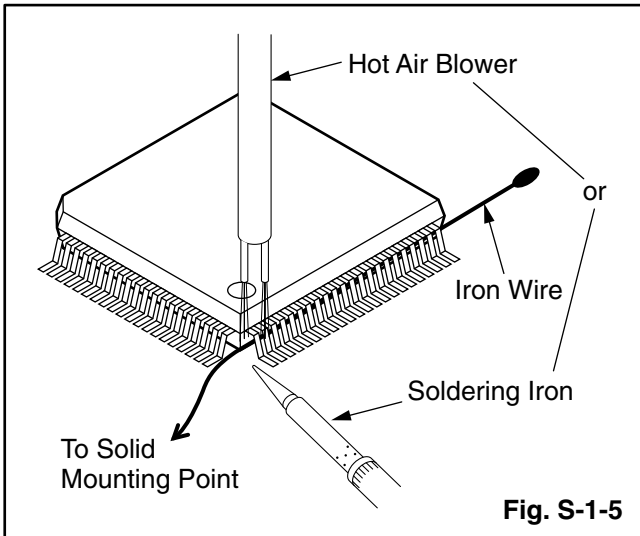


Fig. S-1-5

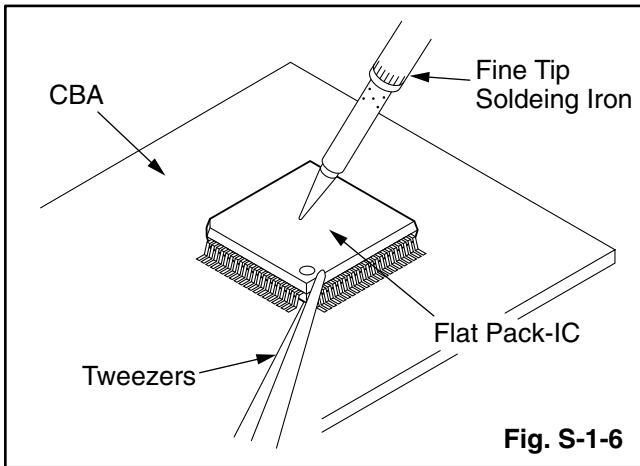


Fig. S-1-6

2. Installation

- (1) Using desoldering braid, remove the solder from the foil of each pin of the flat pack-IC on the CBA so you can install a replacement flat pack-IC more easily.
- (2) The "●" mark on the flat pack-IC indicates pin 1. (See Fig. S-1-7.) Be sure this mark matches the 1 on the PCB when positioning for installation. Then presolder the four corners of the flat pack-IC. (See Fig. S-1-8.)
- (3) Solder all pins of the flat pack-IC. Be sure that none of the pins have solder bridges.

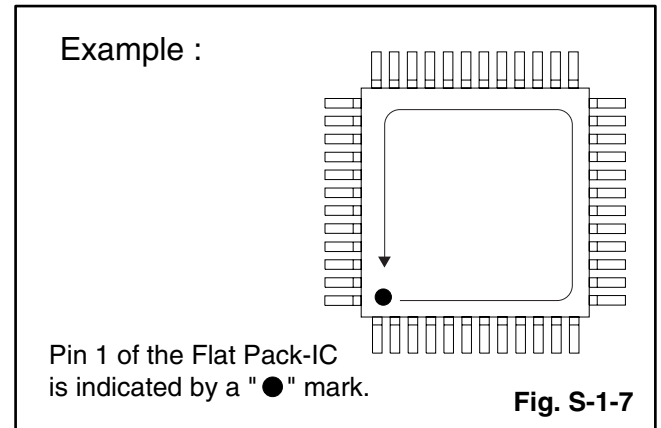


Fig. S-1-7

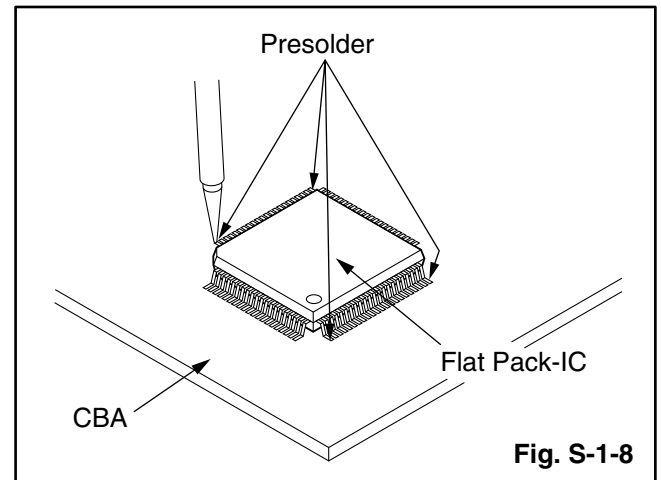


Fig. S-1-8

Instructions for Handling Semi-conductors

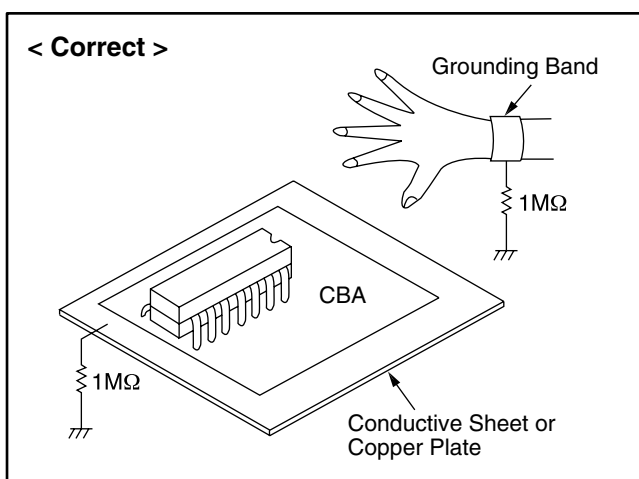
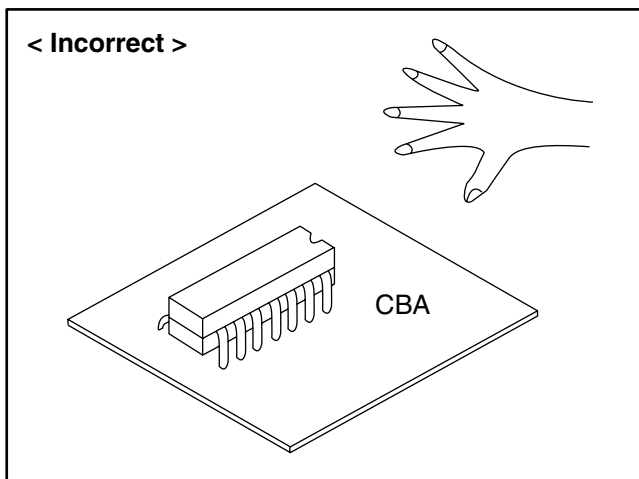
Electrostatic breakdown of the semi-conductors may occur due to a potential difference caused by electrostatic charge during unpacking or repair work.

1. Ground for Human Body

Be sure to wear a grounding band ($1M\Omega$) that is properly grounded to remove any static electricity that may be charged on the body.

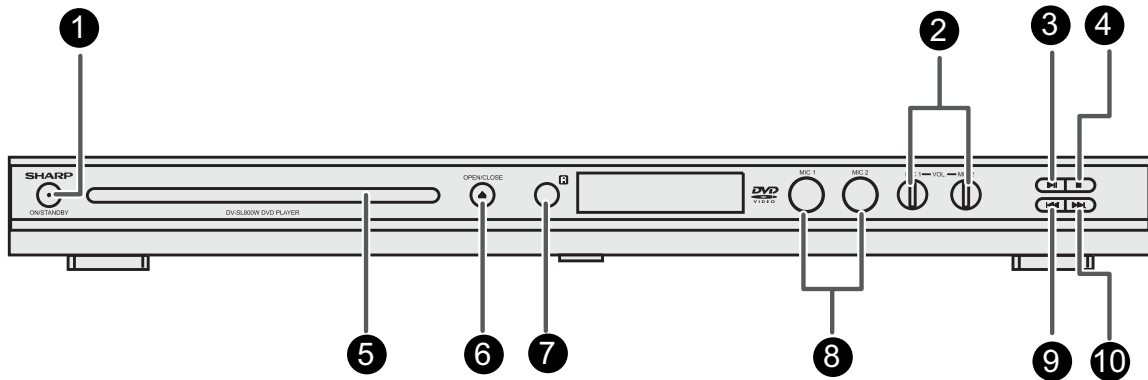
2. Ground for Workbench

Be sure to place a conductive sheet or copper plate with proper grounding ($1M\Omega$) on the workbench or other surface, where the semi-conductors are to be placed. Because the static electricity charge on clothing will not escape through the body grounding band, be careful to avoid contacting semi-conductors with your clothing.



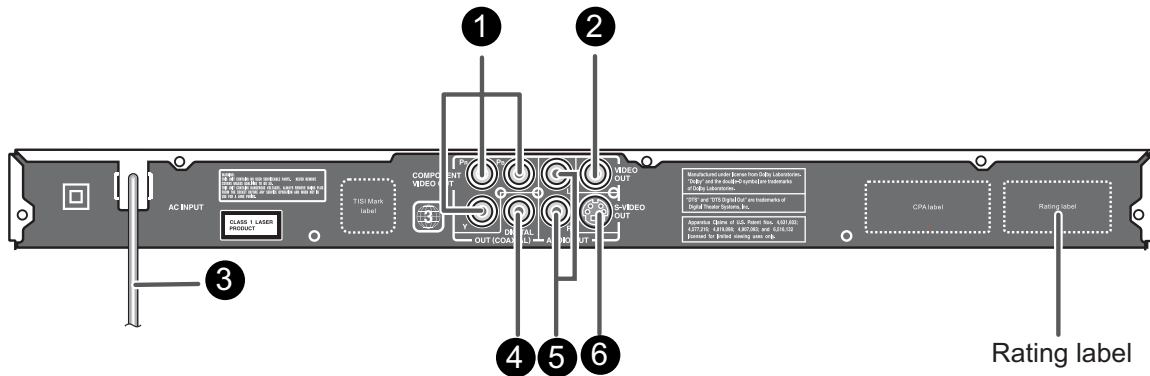
OPERATING CONTROLS AND FUNCTIONS

■ Main unit (front panel)



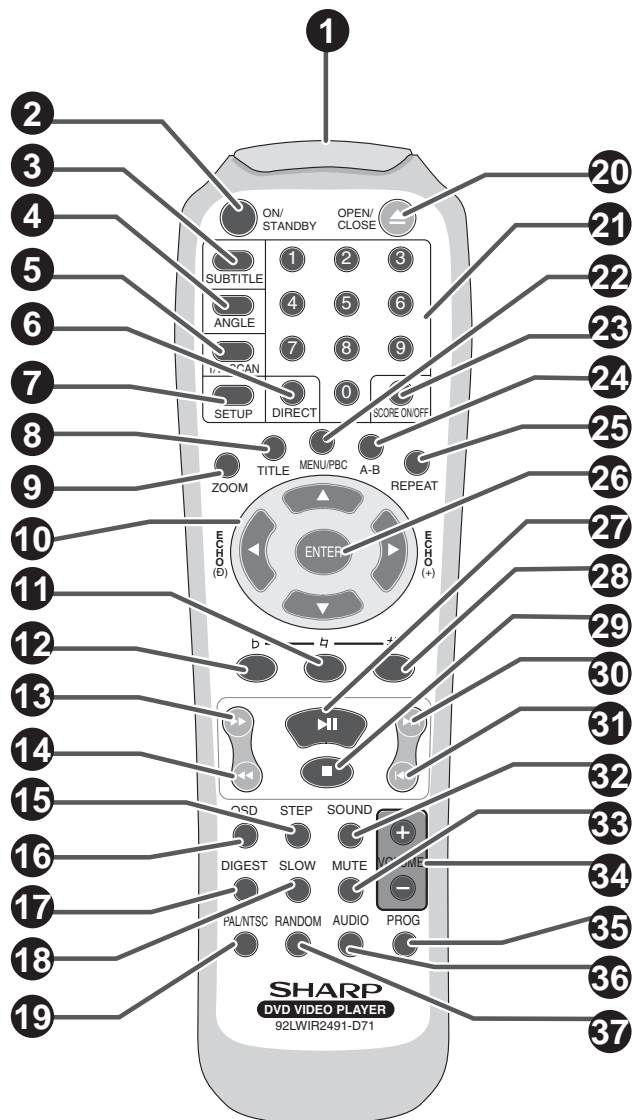
- | | |
|-------------------------------|--------------------------------|
| 1. ON/STANDBY Button | 6. Disc Tray Open/Close Button |
| 2. Microphone Volume Controls | 7. Remote Sensor |
| 3. Play or Pause Button | 8. Microphone Sockets |
| 4. Stop Button | 9. Chapter (track) Skip down |
| 5. Disc Tray | 10. Chapter (track) Skip up |

■ Main unit (rear panel)



1. Component Video Output Sockets
2. Video Output Socket
3. AC Power Lead
4. Digital Output Socket (Coaxial)
5. Audio Output Sockets
6. S-Video Output Socket

■ Remote Control



1. Remote Control Transmitter
2. ON/STANDBY
3. Subtitle Select Button
4. Angle Select Button
5. Interlace and Progressive Scan
6. Direct Button
7. Setup Button
8. Title Select Button
9. Zoom Button
10. Cursor or Echo Level Up and Down Buttons
11. Key Control Button (normal)
12. Key Control Button (lower)
13. Fast Forward
14. Fast Backward
15. Step Button (Frame by frame advance Playback)
16. On screen Display On/Off Button
17. Video CD Digest Button
18. Slow Button
19. PAL/NTSC Select Button
20. Disc Tray Open/Close Button
21. Direct Number Buttons
22. Menu/Playback Control On/Off Button
23. KARAOKE Scoring ON/OFF
24. A-B Repeat Button
25. Repeat Play Button
26. Enter Button
27. Play or Pause Button
28. Key Control Button (highest)
29. Stop Button
30. Chapter (track) Skip Up
31. Chapter (track) Skip Down
32. Sound Button
33. Mute Button
34. Volume Up and Down Buttons
35. Programme Button
36. Audio Select Button
37. Random Button

BLOCK DIAGRAM

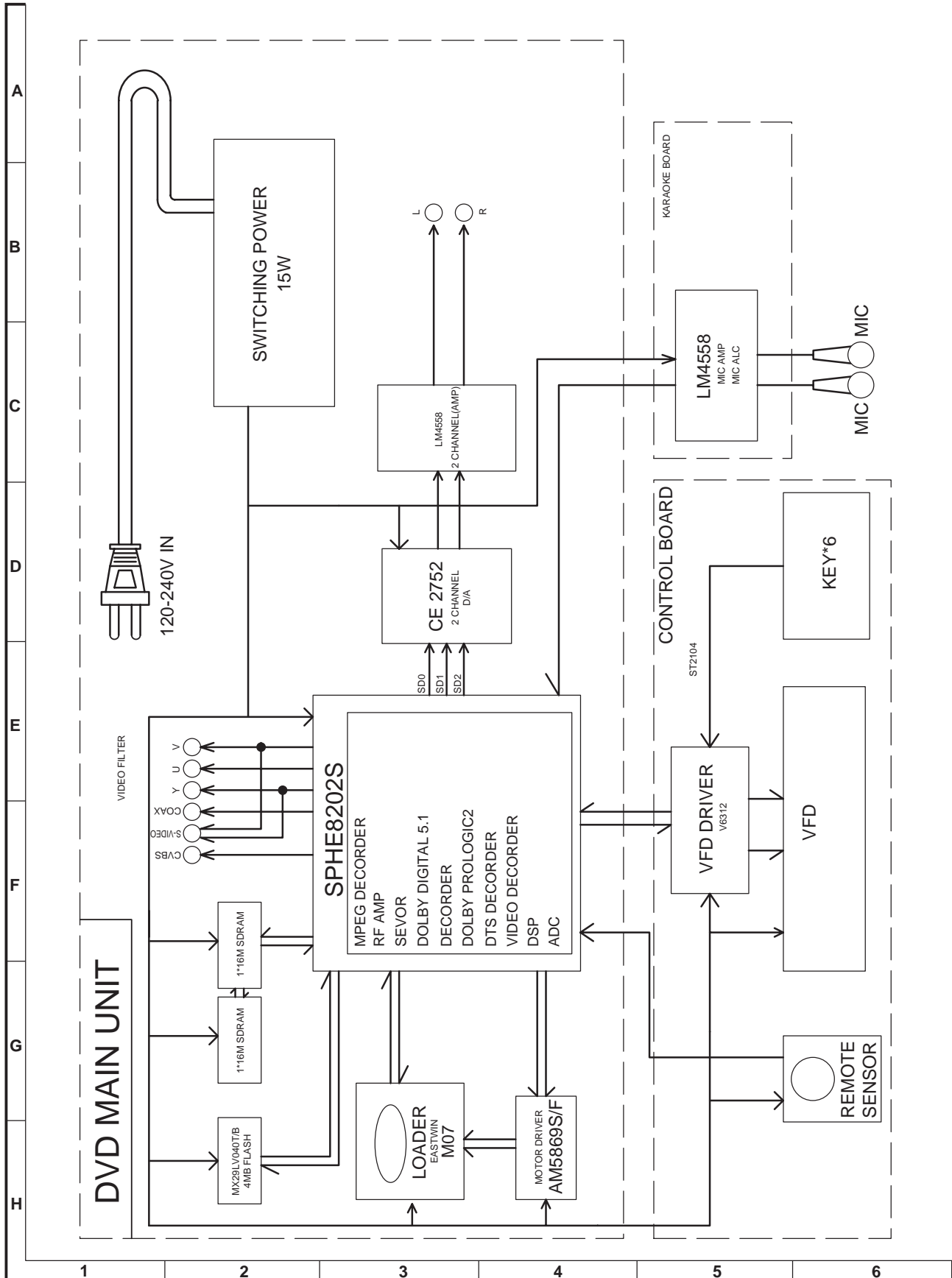


FIGURE 1. BLOCK DIAGRAM

-MEMO-

SCHEMATIC DIAGRAM

POWER PCB SCHEMATIC DIAGRAM

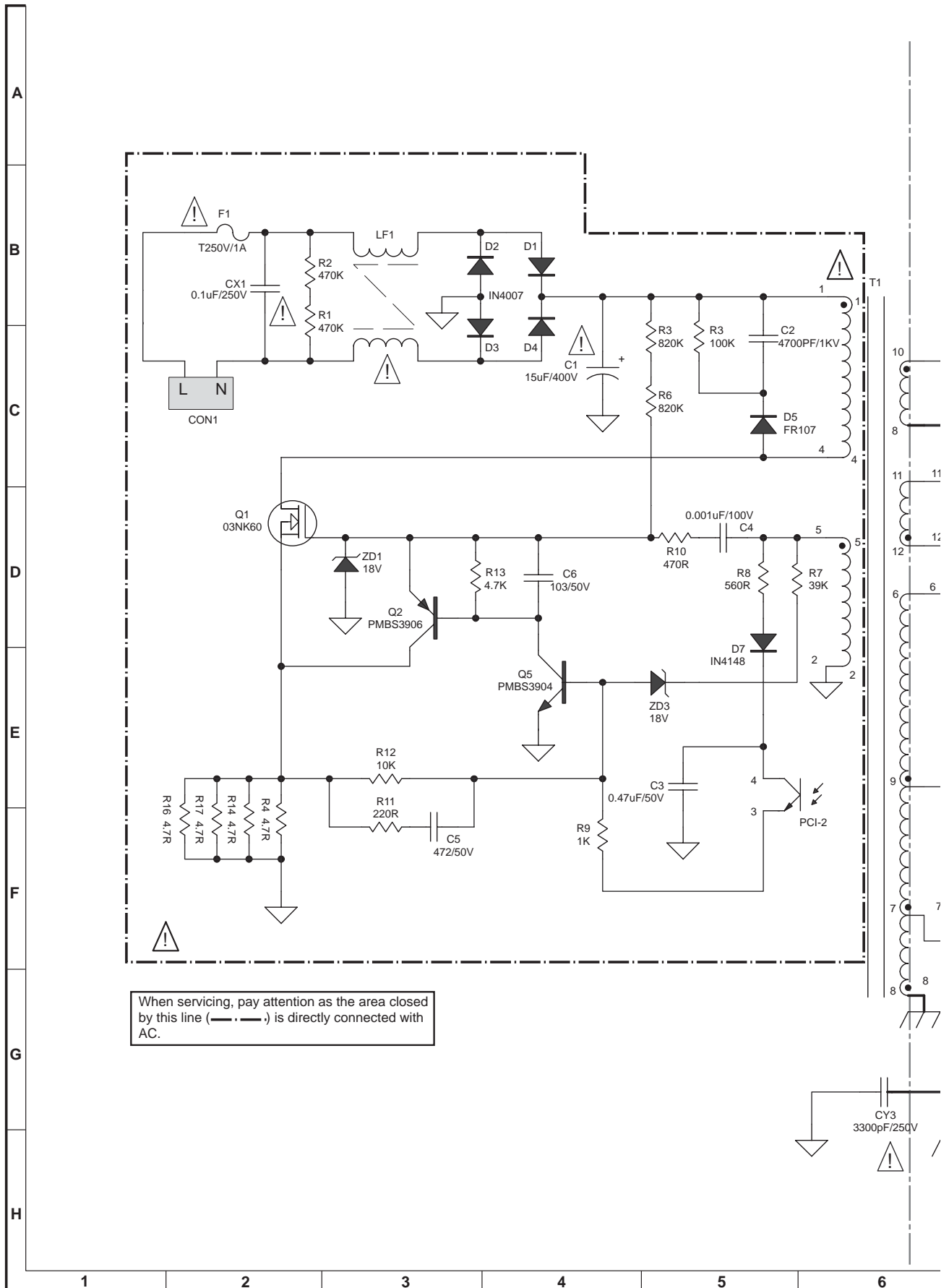


Figure 1: POWER PCB SCHEMATIC DIAGRAM (1/2)

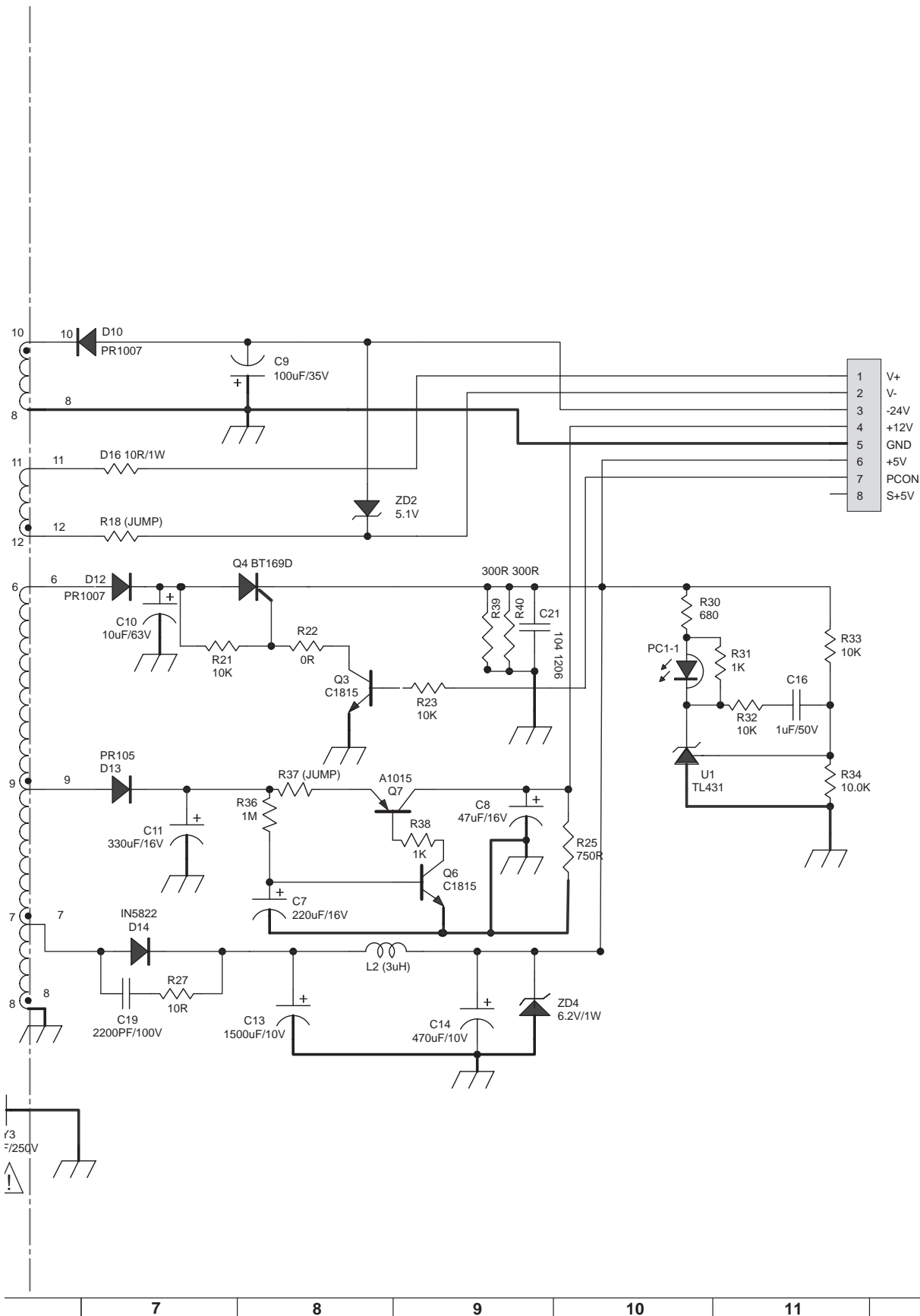


Figure 1: POWER PCB SCHEMATIC DIAGRAM (2/2)

CONTROL PCB SCHEMATIC DIAGRAM

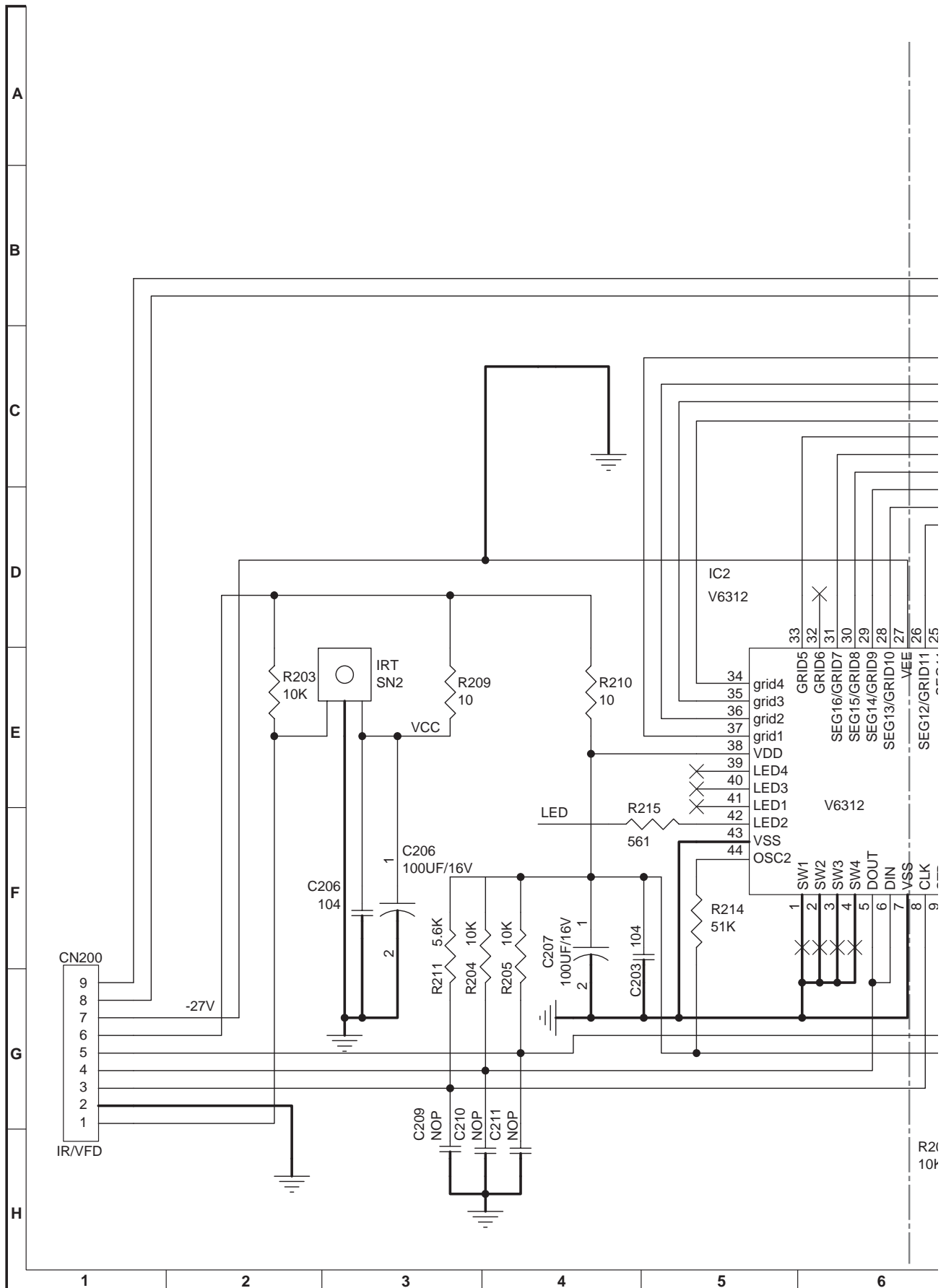


Figure 2: CONTROL PCB SCHEMATIC DIAGRAM (1/2)

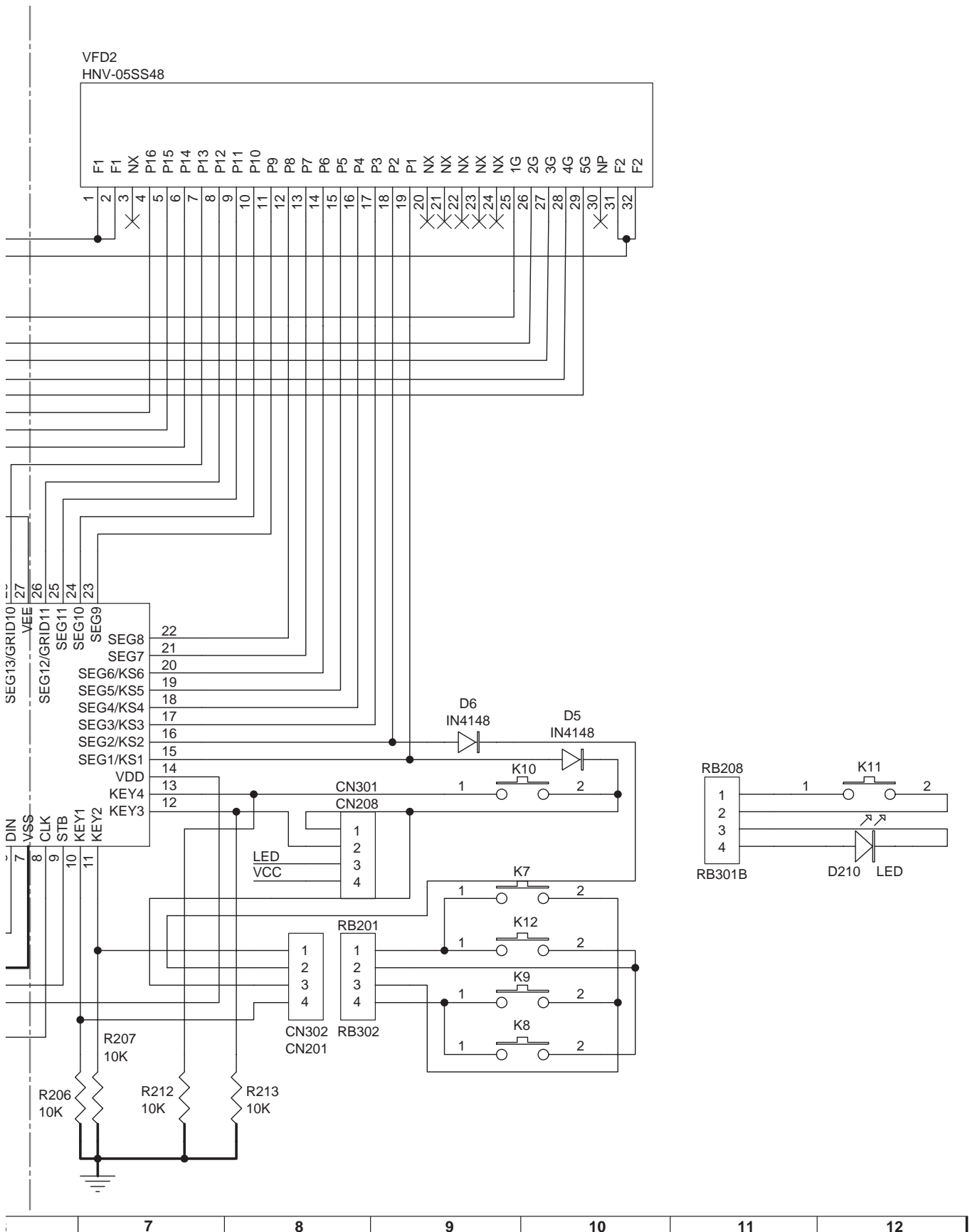


Figure 2: CONTROL PCB SCHEMATIC DIAGRAM (2/2)

KARAOKE PCB SCHEMATIC DIAGRAM

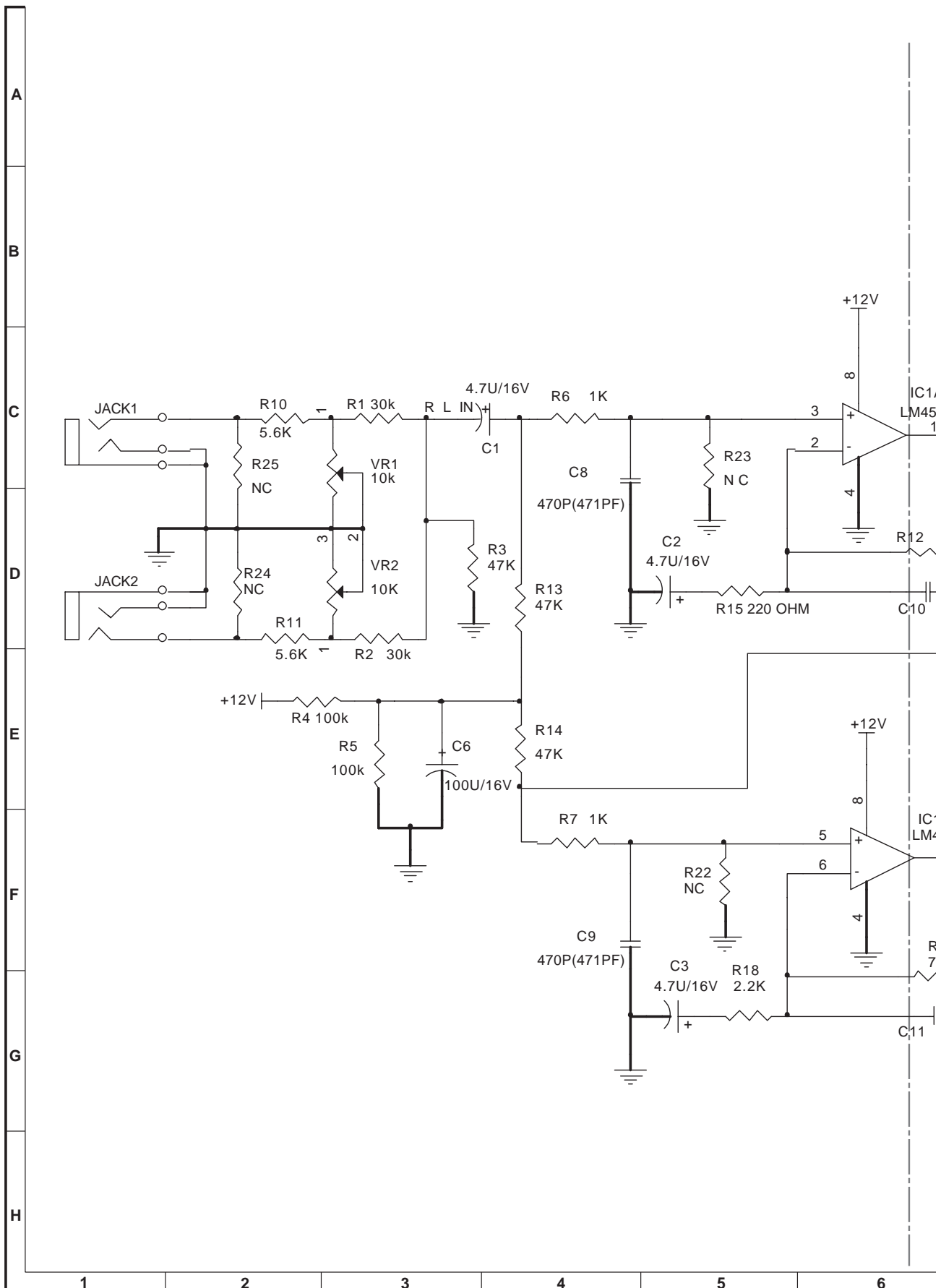


Figure 3: KARAOKE PCB SCHEMATIC DIAGRAM (1/2)

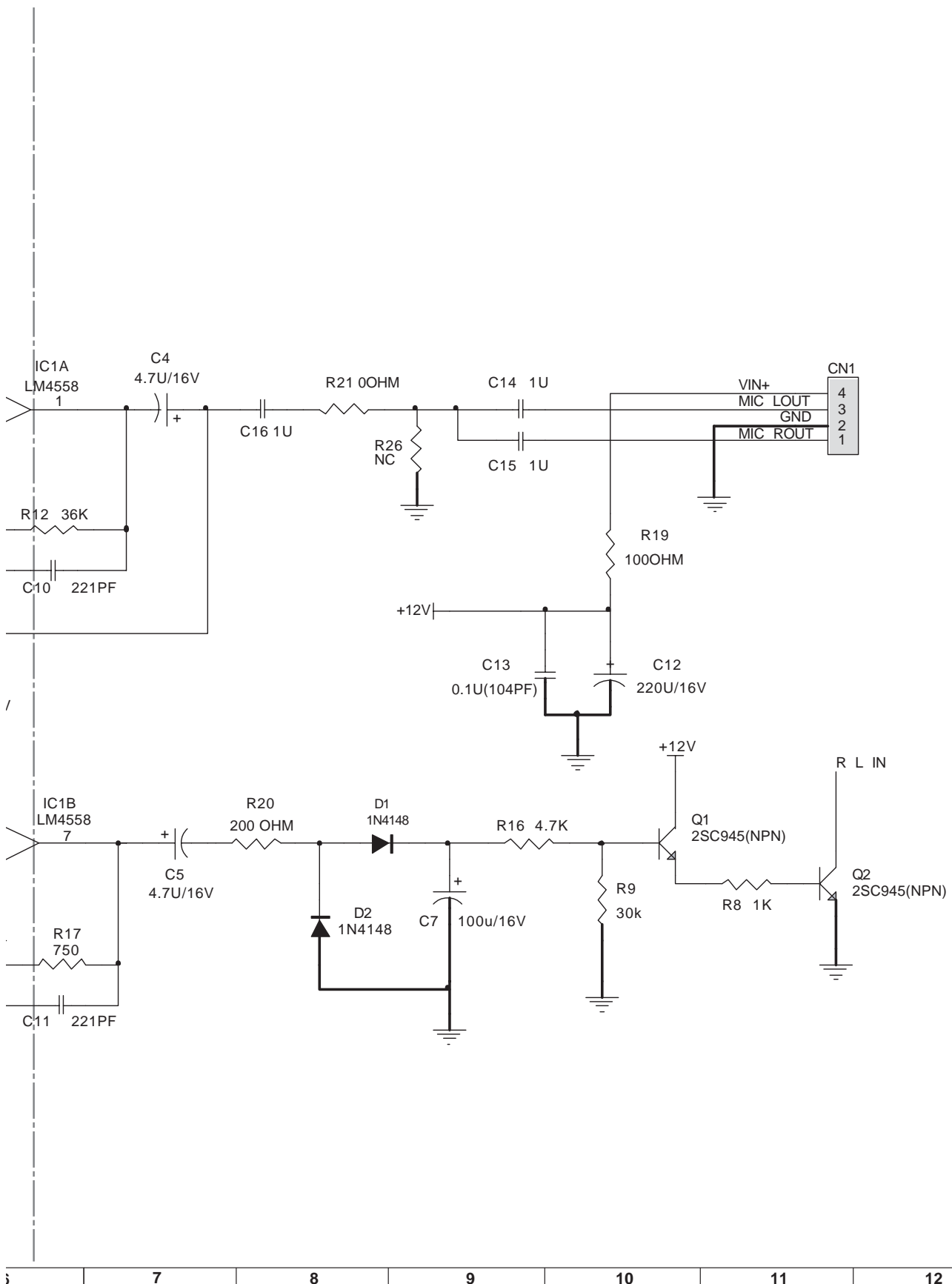


Figure 3: KARAOKE PCB SCHEMATIC DIAGRAM (2/2)

MAIN PCB SCHEMATIC DIAGRAM

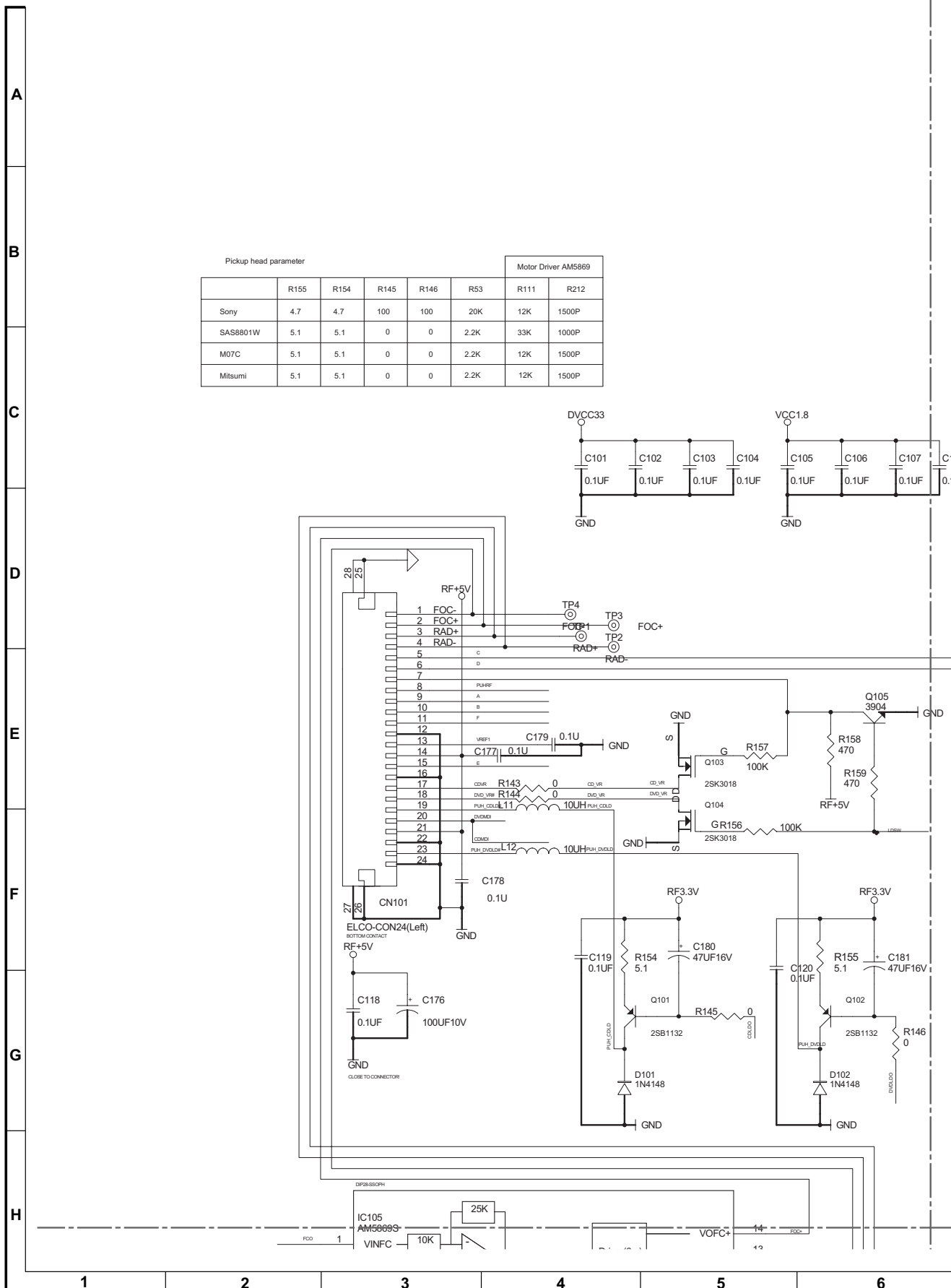


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (1/8)

MAIN PCB SCHEMATIC DIAGRAM

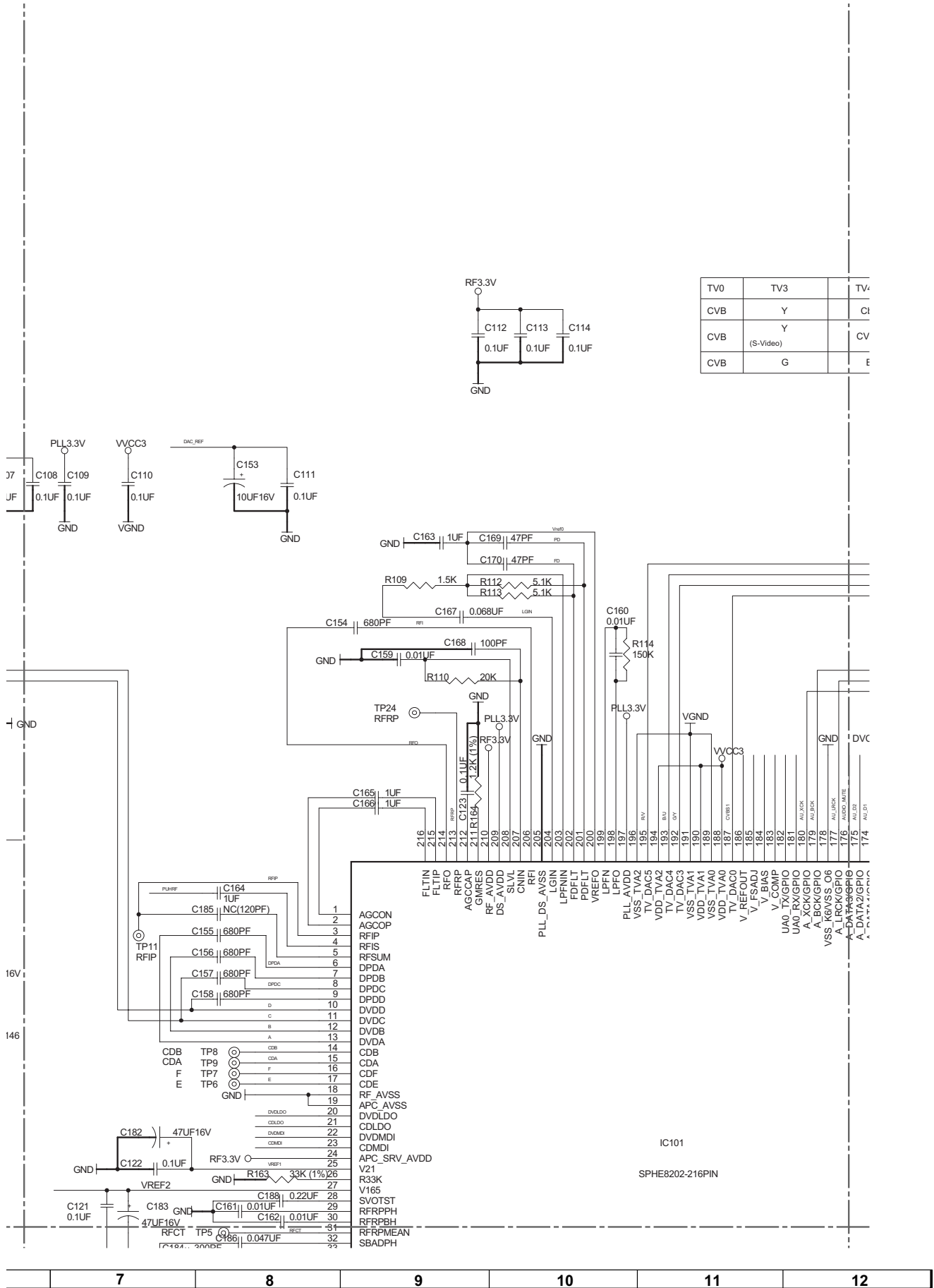


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (2/8)

MAIN PCB SCHEMATIC DIAGRAM

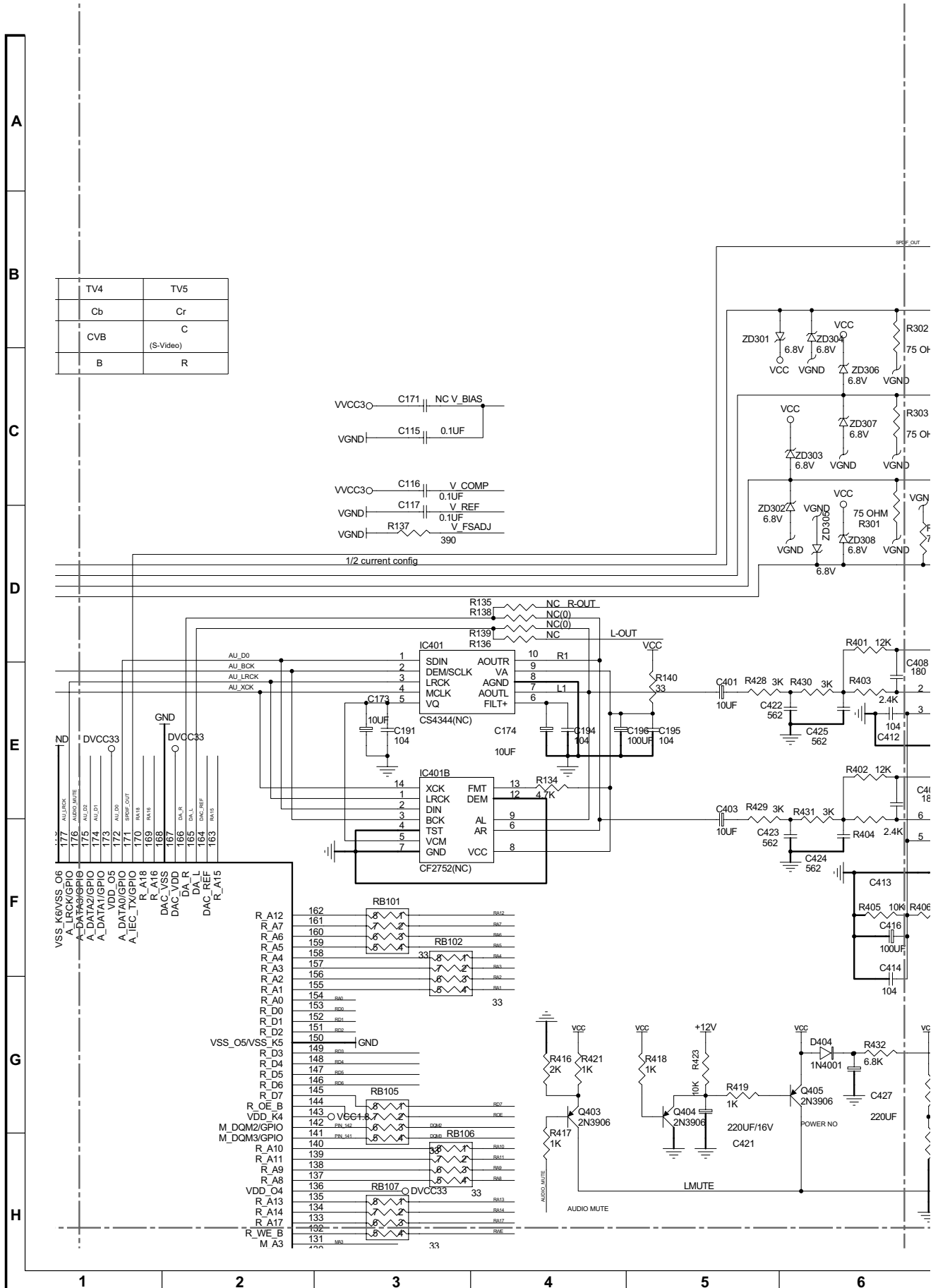


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (3/8)

MAIN PCB SCHEMATIC DIAGRAM

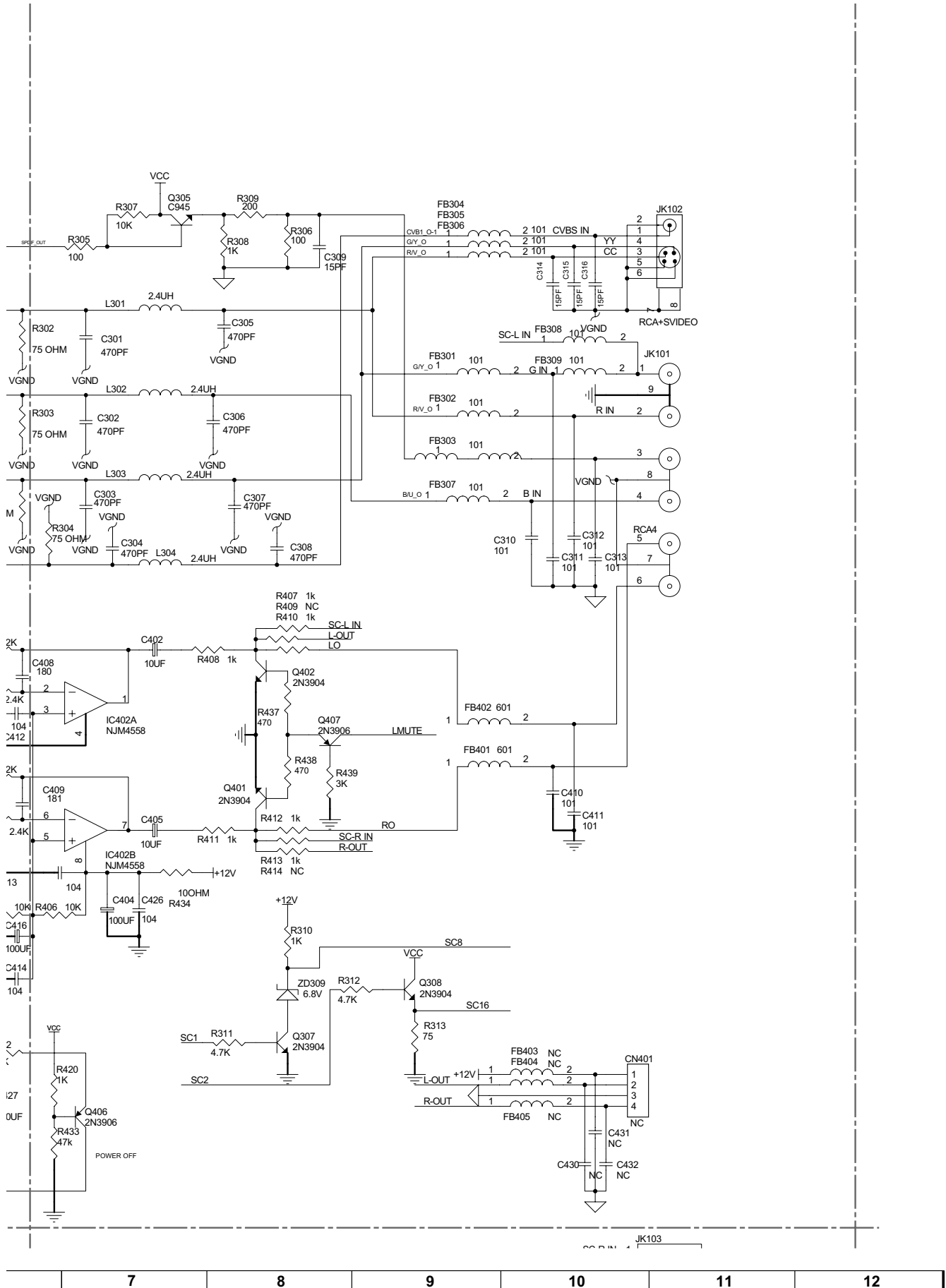


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (4/8)

MAIN PCB SCHEMATIC DIAGRAM

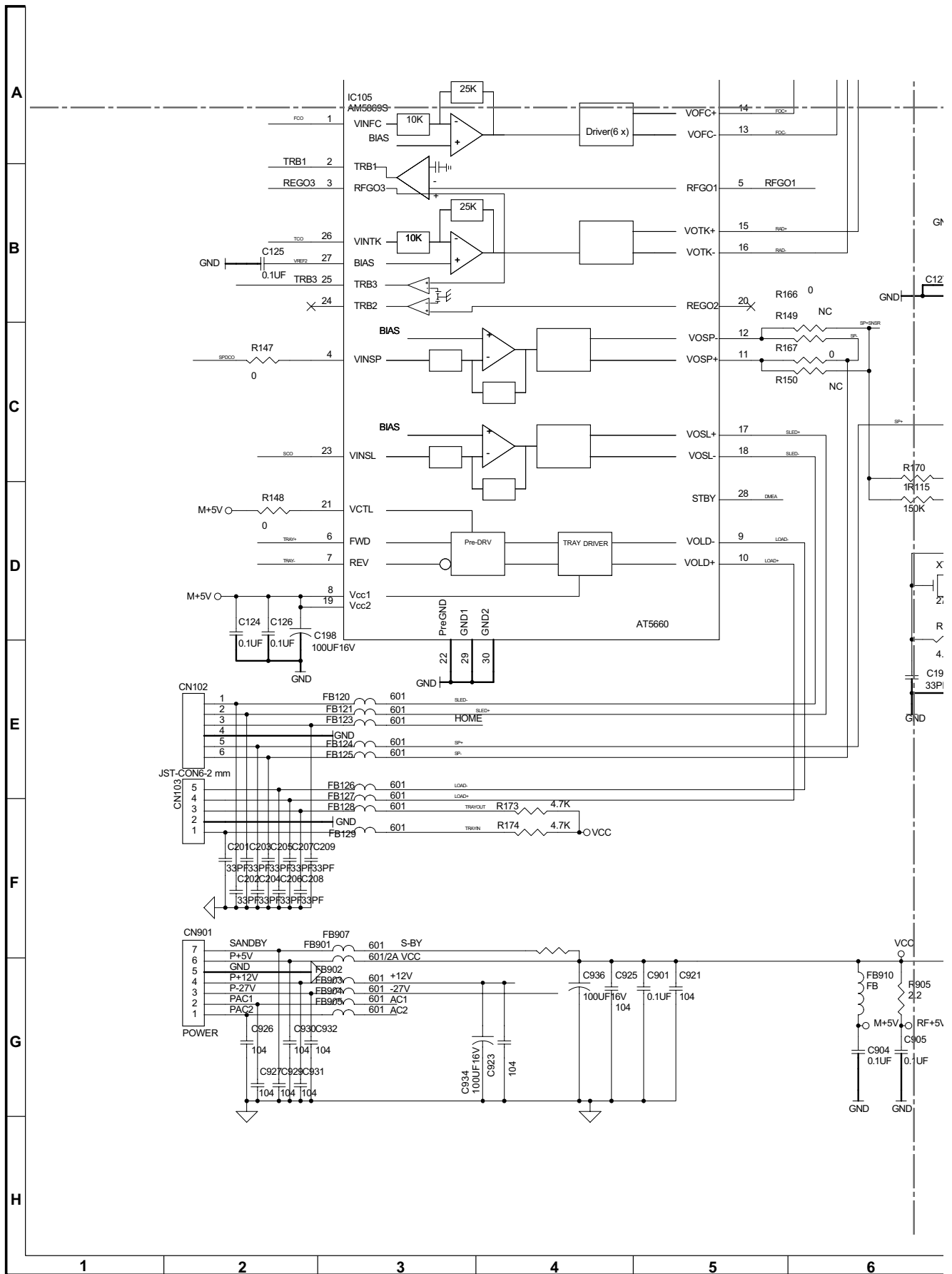


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (5/8)

MAIN PCB SCHEMATIC DIAGRAM

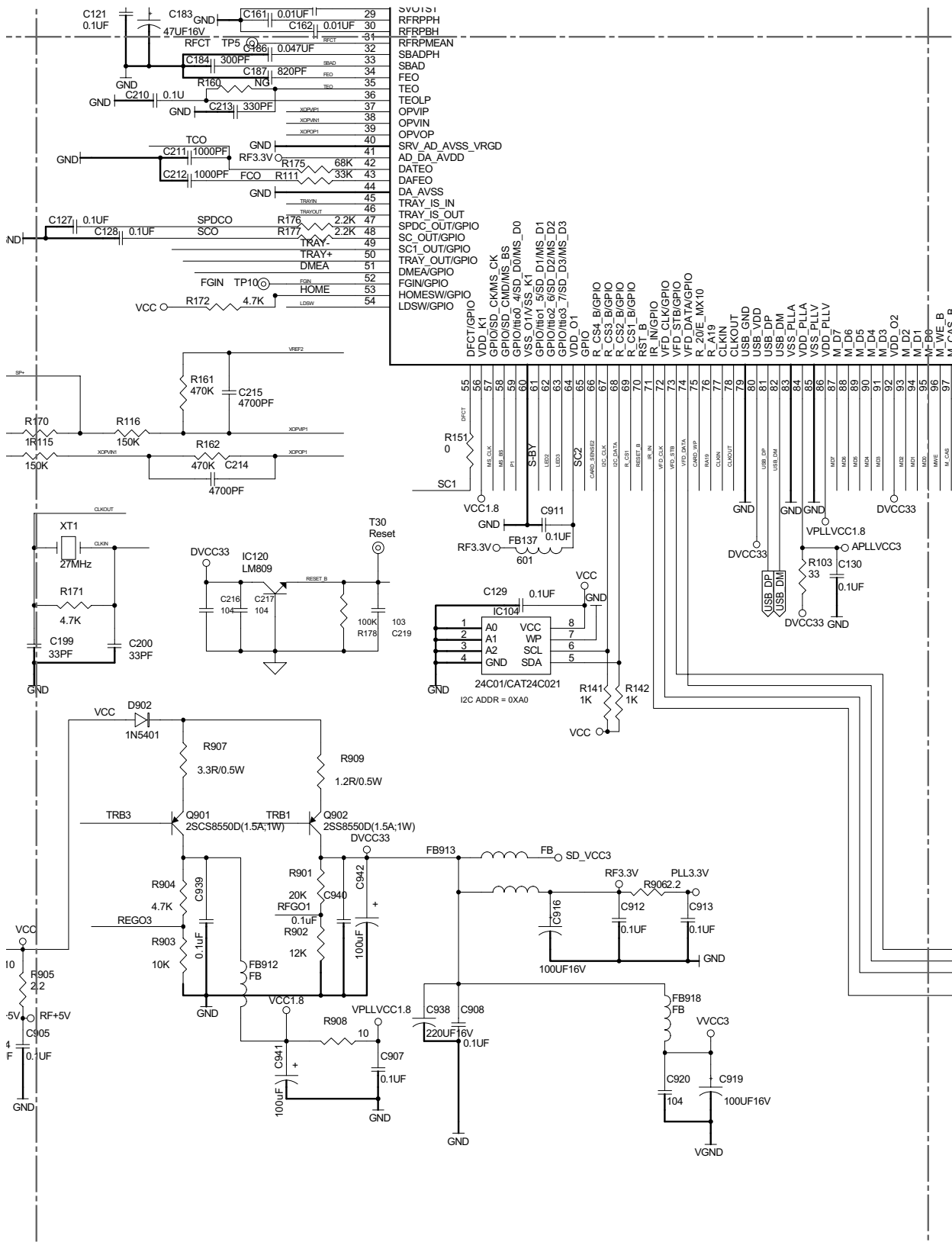


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (6/8)

MAIN PCB SCHEMATIC DIAGRAM

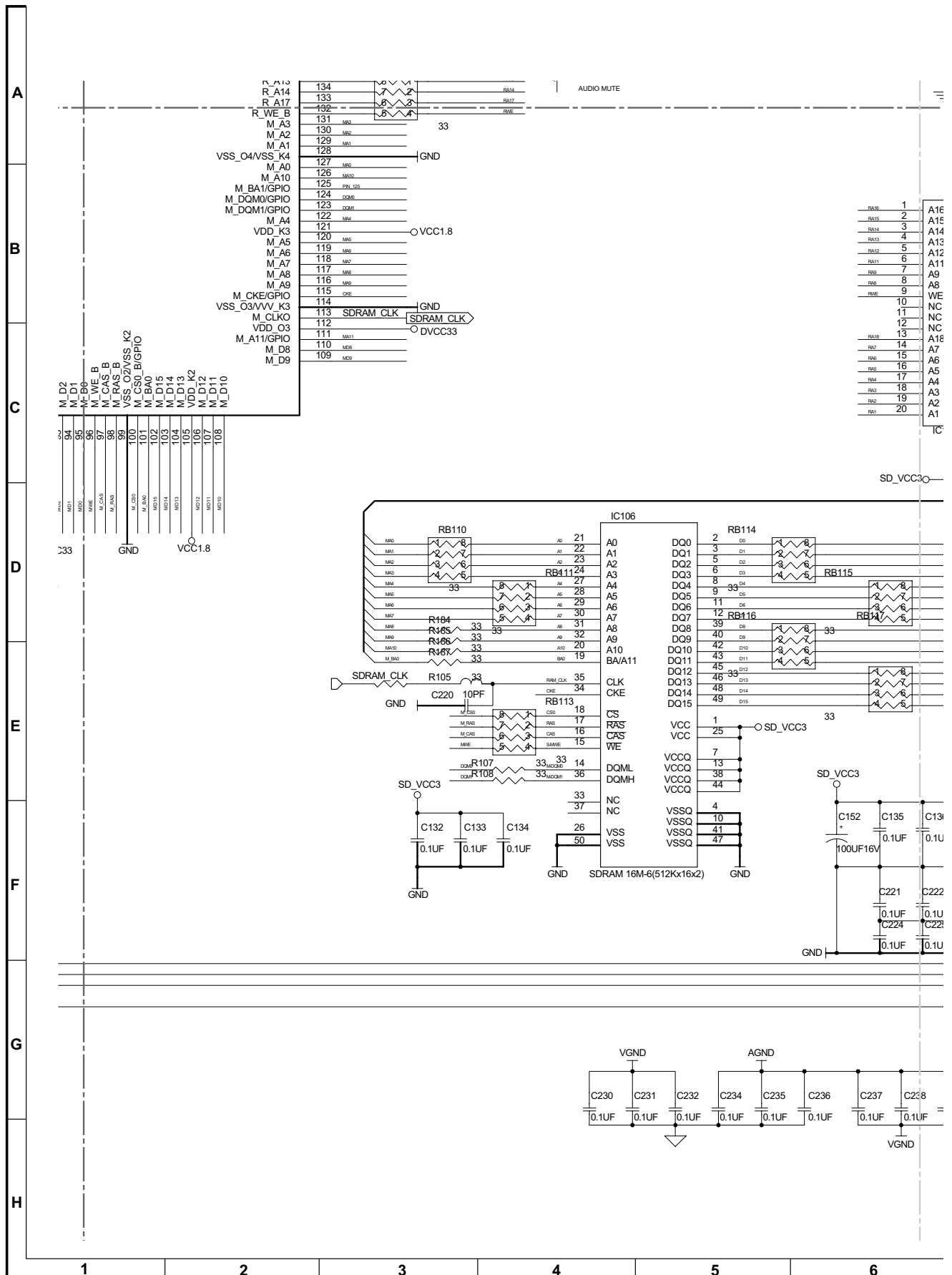


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (7/8)

MAIN PCB SCHEMATIC DIAGRAM

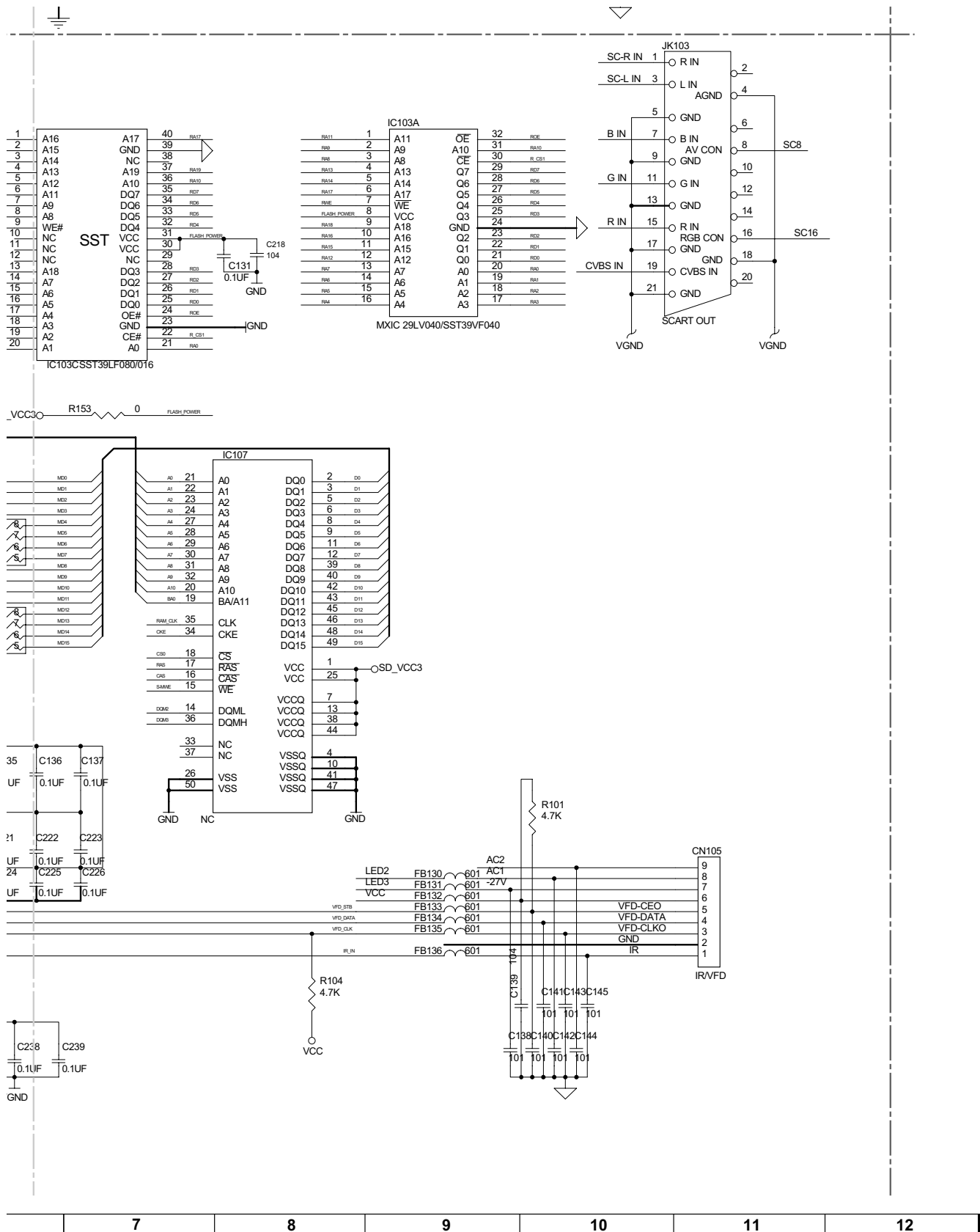


Figure 4: MAIN PCB SCHEMATIC DIAGRAM (8/8)

IC'S PIN VOLTAGE CHART

IC101(SPCA8202S)

Ref.number Mode	1	2	3	4	5	6	7	8	9	10	11	12
	play	0.94	0.95	0.42	2.09	0.95	2.1	2.1	2.1	2.1	2.2	2.2
stop	0.94	0.95	0.44	2.09	0.95	2.1	2.1	2.1	2.1	2.2	2.2	2.2
	13	14	15	16	17	18	19	20	21	22	23	24
play	2.47	1.5	1.5	2.45	1.7	0	0	3.3	2.46	0.19	0.19	3.3
stop	2.47	1.5	1.5	2.45	1.7	0	0	3.3	2.46	0.19	0.19	3.3
	25	26	27	28	29	30	31	32	33	34	35	36
play	2.1	1.67	1.7	1.53	1.95	1.95	1.64	2.02	1.98	1.75	1.86	1.86
stop	2.1	1.68	1.7	1.53	1.95	1.95	1.64	2.02	1.98	1.75	1.86	1.86
	37	38	39	40	41	42	43	44	45	46	47	48
play	2.65	2.7	1.55	0	3.3	1.83	1.7	0	0	5	1.52	1.77
stop	2.65	2.7	1.55	0	3.3	1.83	1.7	0	0	5	1.52	1.77
	49	50	51	52	53	54	55	56	57	58	59	60
play	0	0	3.3	2.1	0	0	0	1.8	2.9	2.83	2.92	0
stop	0	0	3.3	2.1	0	0	0	1.8	2.9	2.83	2.92	0
	61	62	63	64	65	66	67	68	69	70	71	72
play	3.3	3.3	3.3	3.3	2.86	3.3	3.3	3.3	2.8	3.3	5	5
stop	3.3	3.3	3.3	3.3	2.86	3.3	3.3	3.3	2.8	3.3	5	5
	73	74	75	76	77	78	79	80	81	82	83	84
play	5	5	0	0	1.7	1.65	1.65	3.3	1.5	1.53	0	3.26
stop	5	5	0	0	1.7	1.65	1.65	3.3	1.5	1.53	0	3.26
	85	86	87	88	89	90	91	92	93	94	95	96
play	0	1.78	1.66	1	1.3	1.3	1.37	3.3	1.5	1.5	1.58	3.2
stop	0	1.78	0.7	0	0.4	0.3	0.1	3.3	0.4	0.4	0.1	2.9
	97	98	99	100	101	102	103	104	105	106	107	108
play	3.2	3.2	0	2.6	1.38	1.5	1.67	1.8	1.4	0	1.48	1.4
stop	3.1	3	0	1.1	0.5	0.3	0.5	1.8	0.4	0	0.5	0.5
	109	110	111	112	113	114	115	116	117	118	119	120
play	1.04	1.08	0	3.3	1.87	0	0.7	0	0	0	0	0.08
stop	0.29	0.27	0	3.3	1.84	0	1.64	0	0	0.16	0.25	0.13
	121	122	123	124	125	126	127	128	129	130	131	132
play	1.8	0	2.82	2.83	0	0	0	0	0	0	0	3.3
stop	1.8	0.18	2.08	2.09	0	0	0	0.11	0.06	0	0.15	3.3
	133	134	135	136	137	138	139	140	141	142	143	144
play	0.45	1.9	2.3	3.3	2.4	1.5	1.5	2.1	3.3	3.3	1.8	0
stop	0.6	2	0.6	3.3	2.39	0.7	2.34	2.7	3.3	3.3	1.8	0
	145	146	147	148	149	150	151	152	153	154	155	156
play	1.7	0.4	1.6	0.7	0.6	0	1.45	0.9	1.34	0.27	0.2	3.01
stop	1.3	0.4	1.27	0.8	0.53	0	1.54	0.8	1.26	0.08	0.08	3.25
	157	158	159	160	161	162	163	164	165	166	167	168
play	0.26	1.51	2.3	1.7	0	1.26	0.7	1.6	1.58	1.23	3.3	0
stop	0.08	0.9	1.37	0.25	0	0.6	3.2	0.4	1.58	1.58	3.3	0

	169	170	171	172	173	174	175	176	177	178	179	180
play	0.3	2.7	0	1.25	3.3	1.26	0	2.88	1.67	0	1.66	1.67
stop	0.9	2.27	0	0	0	0	0	2.88	1.67	0	1.66	1.67
	181	182	183	184	185	186	187	188	189	190	191	192
play	0.62	3.3	0.6	0.6	0.59	1.21	0.52	3.29	0	3.29	0	1.07
stop	0.62	3.3	0	0.6	0.59	1.21	0.52	3.29	0	3.29	0	1.08
	193	194	195	196	197	198	199	200	201	202	203	204
play	1.17	3.29	1.2	0	3.26	0.03	2.64	1.67	1.67	1.67	1.68	1.46
stop	1.17	3.29	1.2	0	3.26	0.3	2.64	1.67	1.67	1.67	1.68	1.46
	205	206	207	208	209	210	211	212	213	214	215	216
play	0	1.68	1.65	1.65	3.26	3.3	0.4	1.61	1.79	0.89	2.38	2.38
stop	0	1.68	1.65	1.65	3.26	3.3	0.4	1.61	1.8	0.89	2.38	2.38

IC105(AM5869)

Ref.number Mode	1	2	3	4	5	6	7	8	9	10	11	12
play	1.66	3.44	1.25	1.44	1.26	0	0	5	0	0	1.25	3.53
stop	1.66	3.44	1.25	1.44	1.26	0	0	5	0	0	1.4	3.4
	13	14	15	16	17	18	19	20	21	22	23	24
play	2.33	2.52	2.45	2.38	2.58	2.18	5	2.35	5	0	1.74	4.86
stop	2.33	2.52	2.54	2.25	2.6	2.2	5	2.3	5	0	1.74	4.86
	25	26	27	28								
play	2.8	1.67	1.67	3.3								
stop	2.8	1.69	1.69	3.3								

IC103A(MX29LV040TC-707)

Ref.number Mode	1	2	3	4	5	6	7	8	9	10	11	12
play	0.9~1.6	2.7	0.6	0.4	1.5~2.5	0.2~0.9	3.28	3.28	0	0.15~0.3	3	0.15
stop	2.9	0.3	0.7	0.6	3	0	3.28	3.28	0	0.58	2.8	0
	13	14	15	16	17	18	19	20	21	22	23	24
play	1	1.8~3.21	1.5~2.4	0.2~1.7	0	3.2	0	0	1.7	1.3	1.9	0
stop	0.98	0.68	0.68	2.3	0	3.23	0	0	0.8	1.8	1.8	0
	25	26	27	28	29	30	31	32				
play	1.3	1.4	1.9	1.6	1.6	1.3	0	3.28				
stop	0.8	0.8	1.8	1.5	1.4	0.6	3.2	3.2				

IC106(1X16Y3VTW-7)

Ref.number Mode	1	2	3	4	5	6	7	8	9	10	11	12
play	3.27	1.2	1.3	0	1.1	1.3	3.27	1.2	1.12	0	1.3	1.6
stop	3.27	0.23	0.23	0	0.25	0.23	3.27	0.21	0.18	0	0.18	0.26
	13	14	15	16	17	18	19	20	21	22	23	24
play	3.27	2.9	3.2	3.1	3.1	2.6	0	0	0	0	0	0
stop	3.27	2.55	2.96	2.98	2.86	1.45	0.3	0	0	0	0	0.16
	25	26	27	28	29	30	31	32	33	34	35	36
play	3.27	0	0	0	0	0	0	0	0	0.7	1.65	2.9

DV-SL800W

stop	3.27	0	0.14	0.1	0.1	0	0	0	0	1.25	1.6	2.55
	37	38	39	40	41	42	43	44	45	46	47	48
play	0	3.27	1.3	1.39	0	1.4	1.4	3.27	1.39	1.25	0	1.49
stop	0	3.27	0.24	0.22	0	0.22	0.22	3.27	0.19	0.18	0	0.16
	49	50										
play	1.13	0										
stop	0.18	0										

IC402(AZ4558)

Ref.number								
Mode	1	2	3	4	5	6	7	8
play	0	0	0	-11.53	0	0	0	11.82
stop	0	0	0	-11.53	0	0	0	11.82

IC104(24C02)

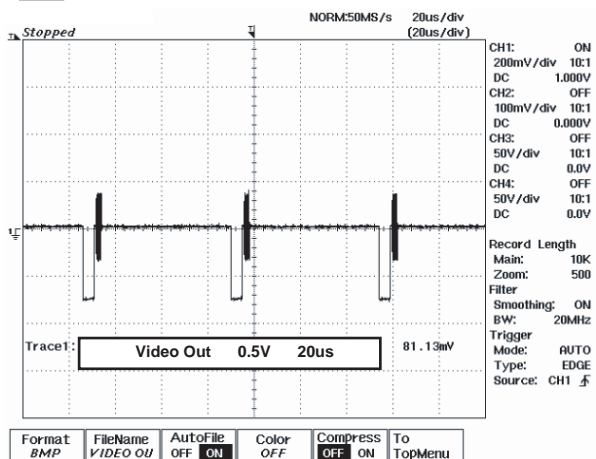
Ref.number								
Mode	1	2	3	4	5	6	7	8
play	0	0	0	0	3.3	3.33	0	4.88
stop	0	0	0	0	3.3	3.33	0	4.88

IC120(ASM809)

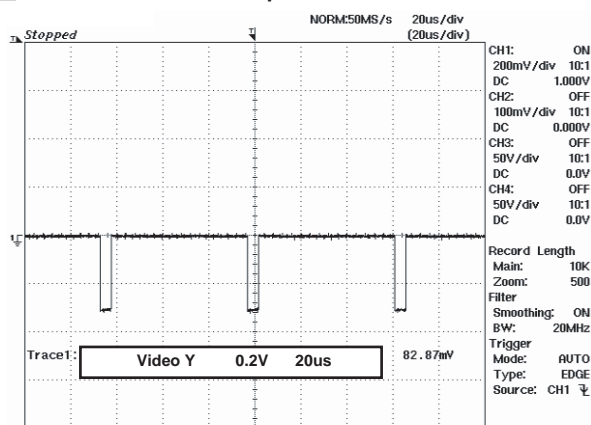
Ref.number			
Mode	1	2	3
play	3.28	0	3.26
stop	3.28	0	3.26

WAVEFORMS

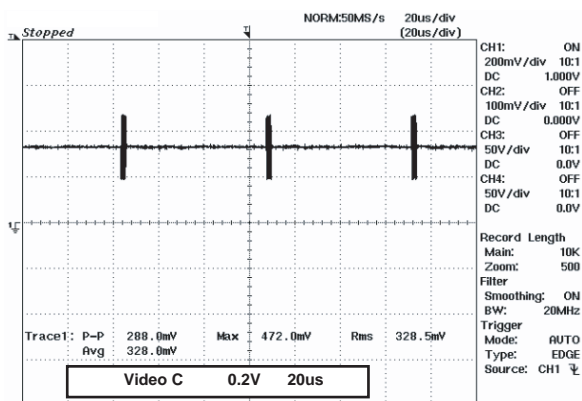
WF1 VIDEO OUT



WF2 S-VIDEO OUT - Y Output



WF3 S-VIDEO OUT - C Output

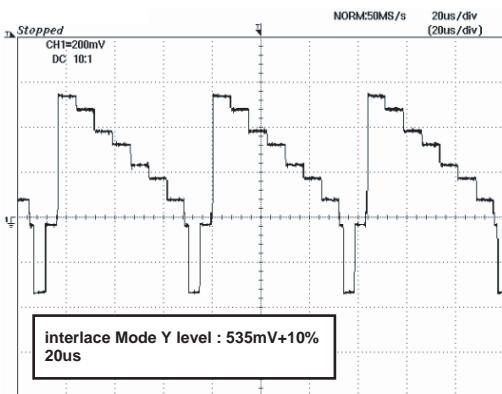


Note :

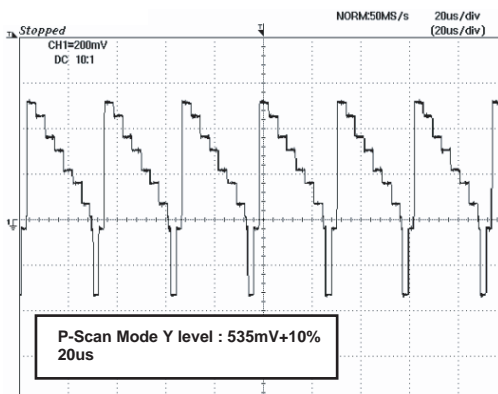
WF1 ~ WF3 : Power On (Stop) Mode.

WF4 ~ WF7 : DVD Test Disc TDV-540A. (Color Bar 75%)

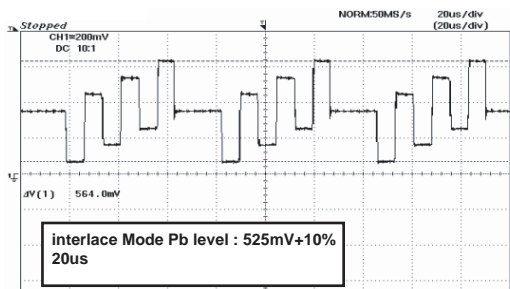
WF4 COMPONENT VIDEO OUT - Y Output (Interlace mode)



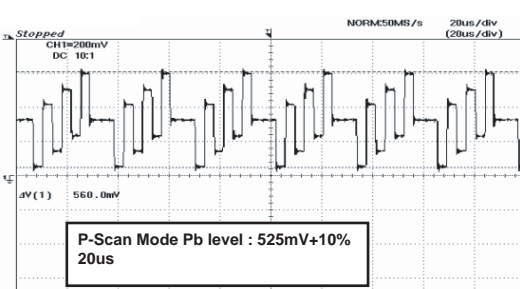
WF5 COMPONENT VIDEO OUT - Y Output (P-Scan mode)



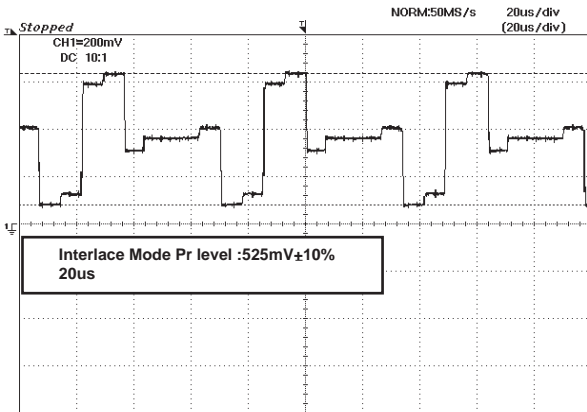
WF6 COMPONENT VIDEO OUT - Pb/Cb Output (Interlace mode)



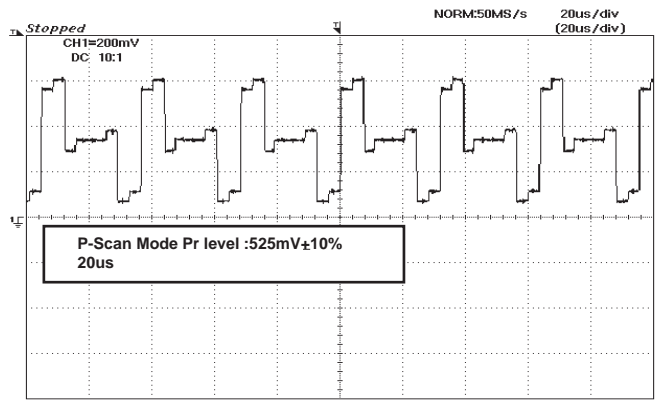
WF7 COMPONENT VIDEO OUT - Pb/Cb Output (P-Scan mode)



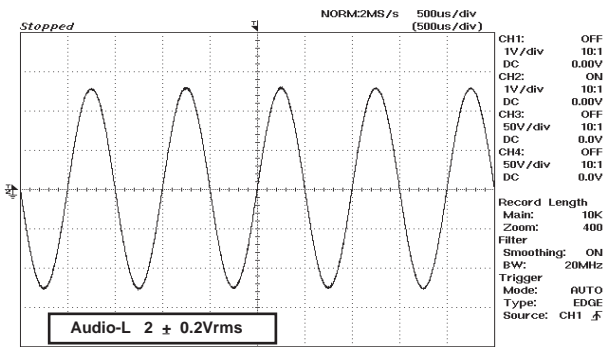
WF8 COMPONENT VIDEO OUT - Pr/Cr Output (Interlace mode)



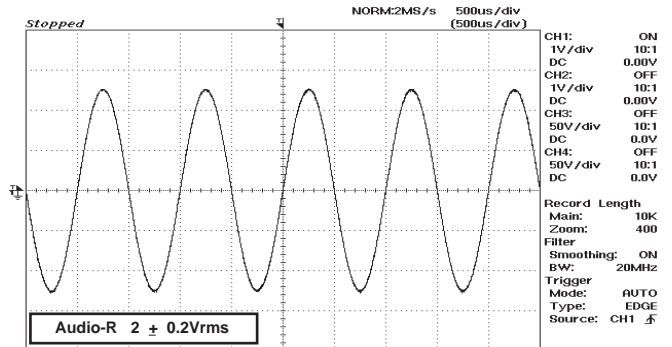
WF9 COMPONENT VIDEO OUT - Pr/Cr Output (P-Scan mode)



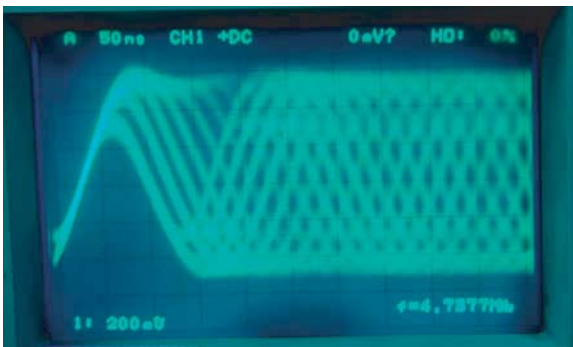
WF10 Audio Left



WF11 Audio Right



WF12 Rf Signal



Note :

WF8 ~ WF9 : DVD Test Disc TDV-540A. (Color Bar 75%)

WF10 ~ WF11 : DVD/CD Test Disc 1KHz, 0dB.

WF12 : Normal Disc.

-MEMO-

OVERALL WIRING CONNECTION

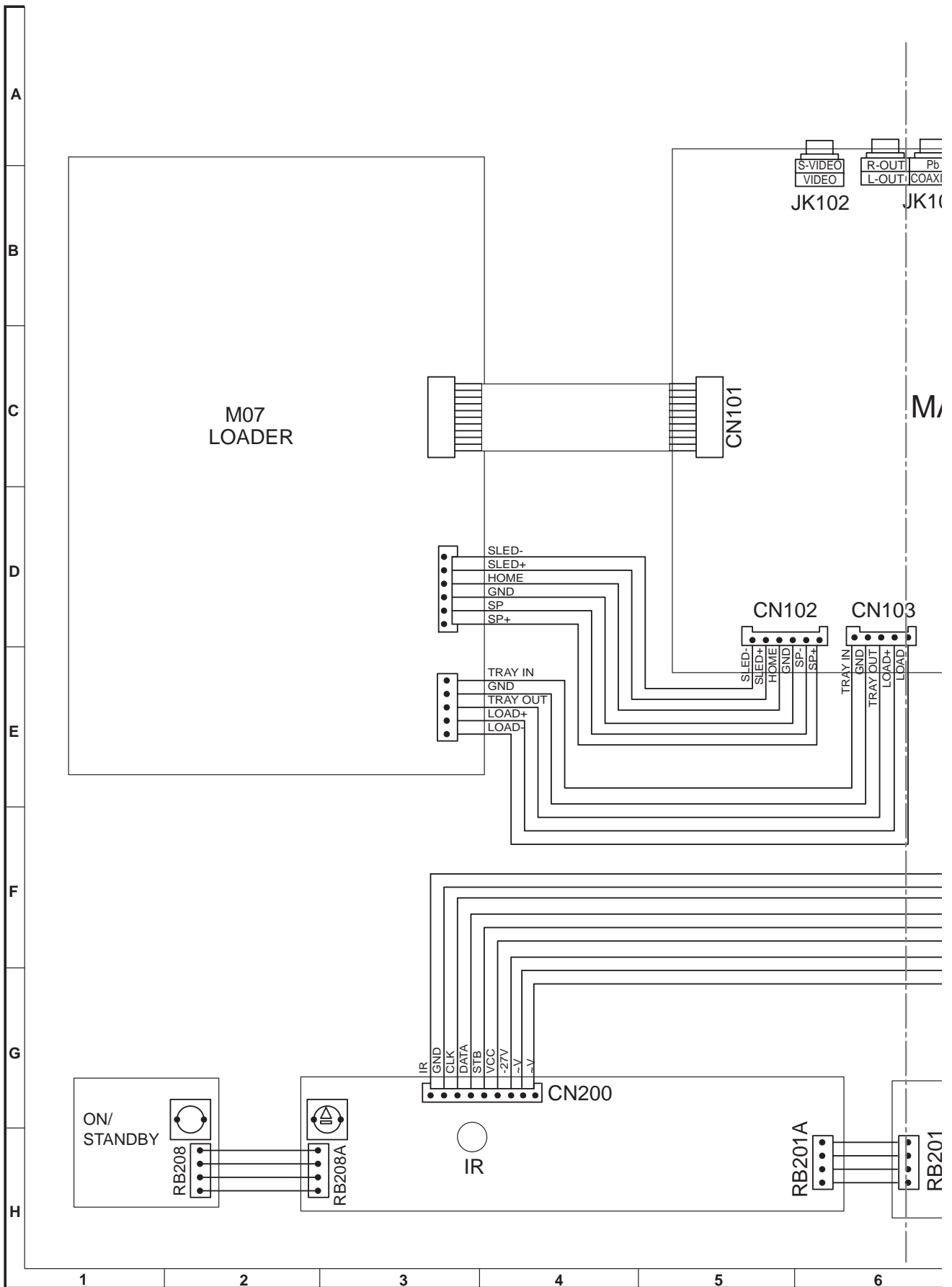


Figure 1: OVERALL WIRING CONNECTION (1/2)

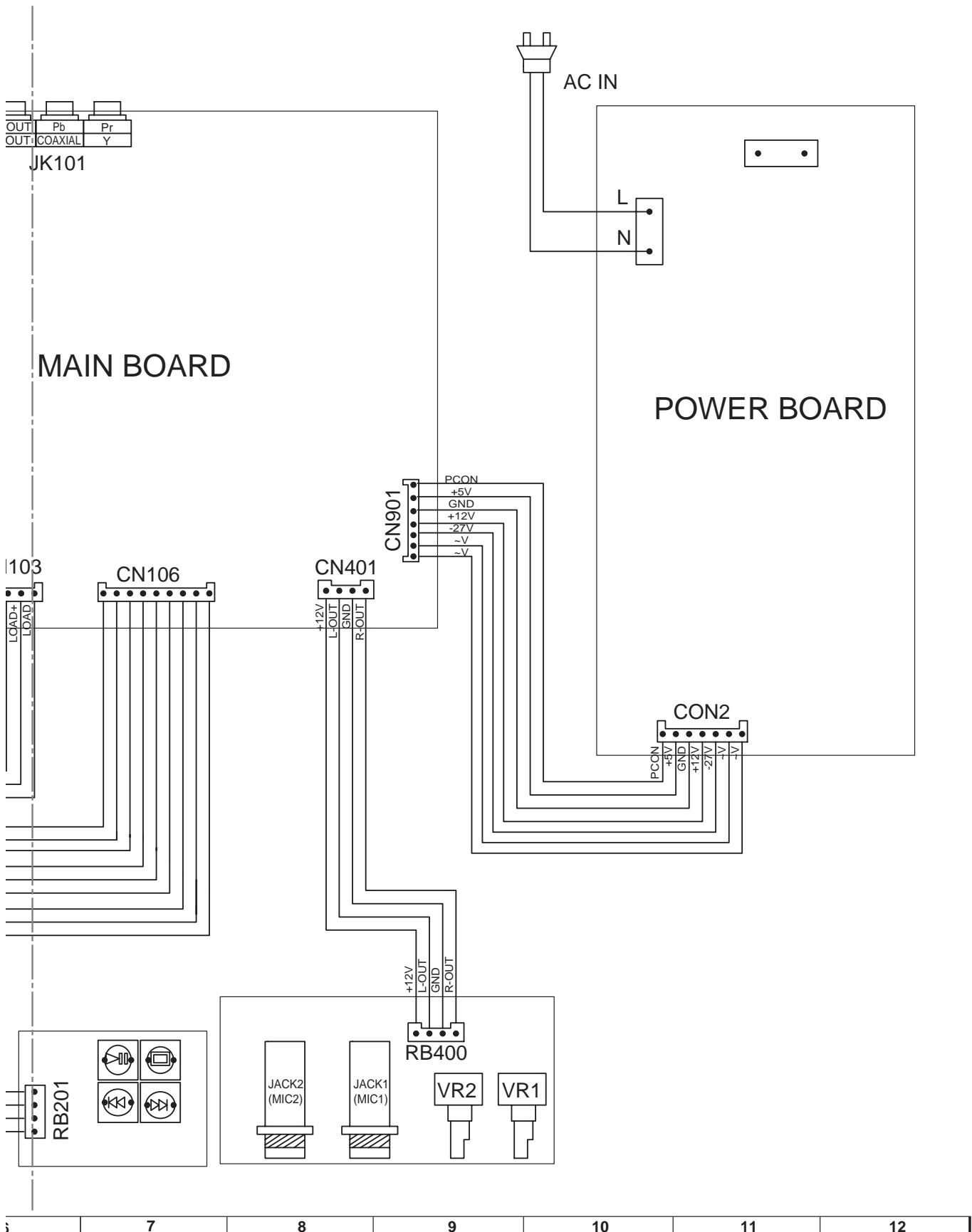


Figure 1: OVERALL WIRING CONNECTION (2/2)

WIRING DIAGRAM

WIRING SIDE OF POWER PCB (TOP VIEW)

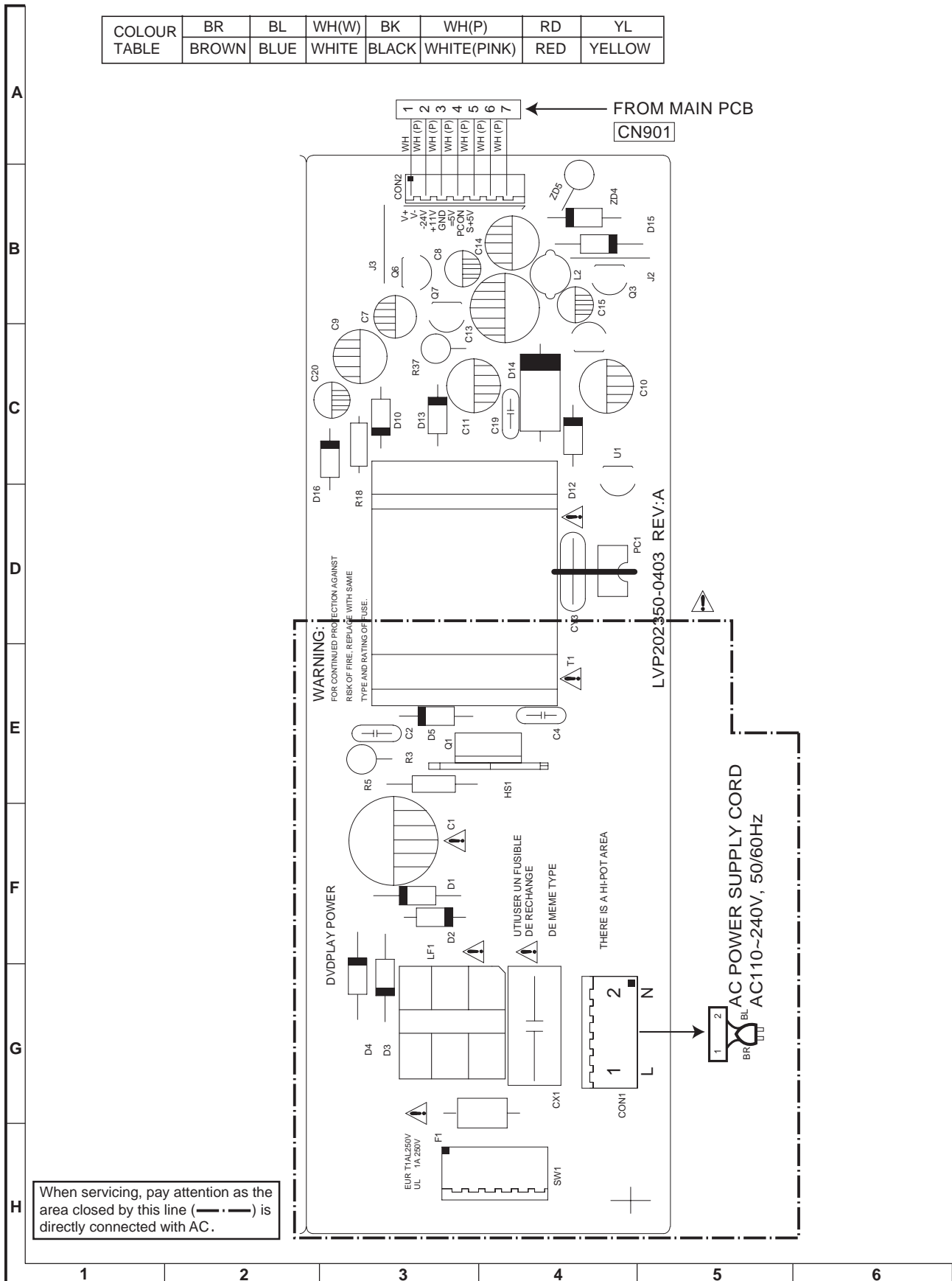


Figure 1: WIRING SIDE OF POWER PCB (TOP VIEW)

WIRING SIDE OF POWER PCB (BOTTOM VIEW)

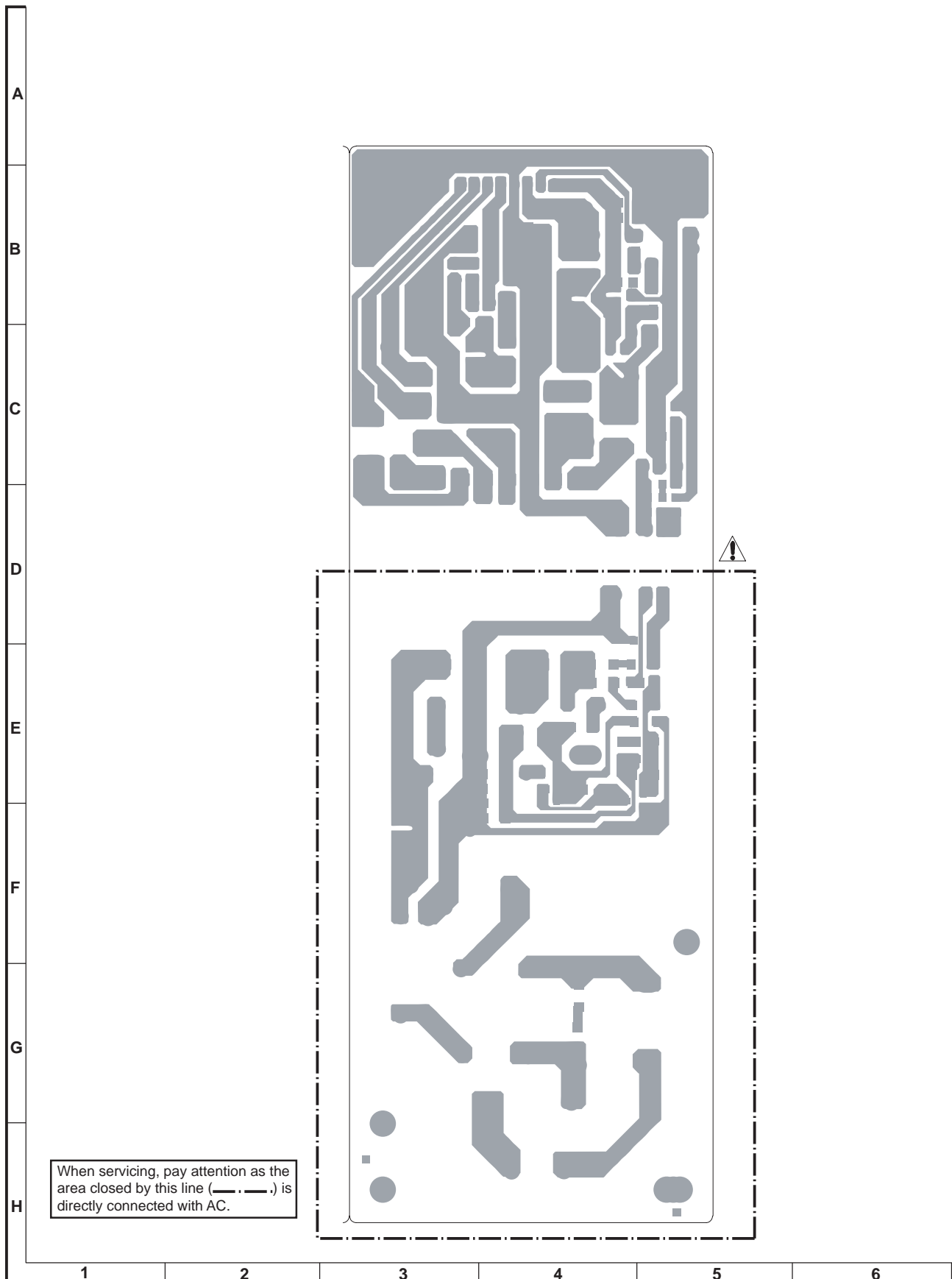


Figure 1: WIRING SIDE OF POWER PCB (BOTTOM VIEW)

WIRING SIDE OF MAIN PCB (TOP VIEW)

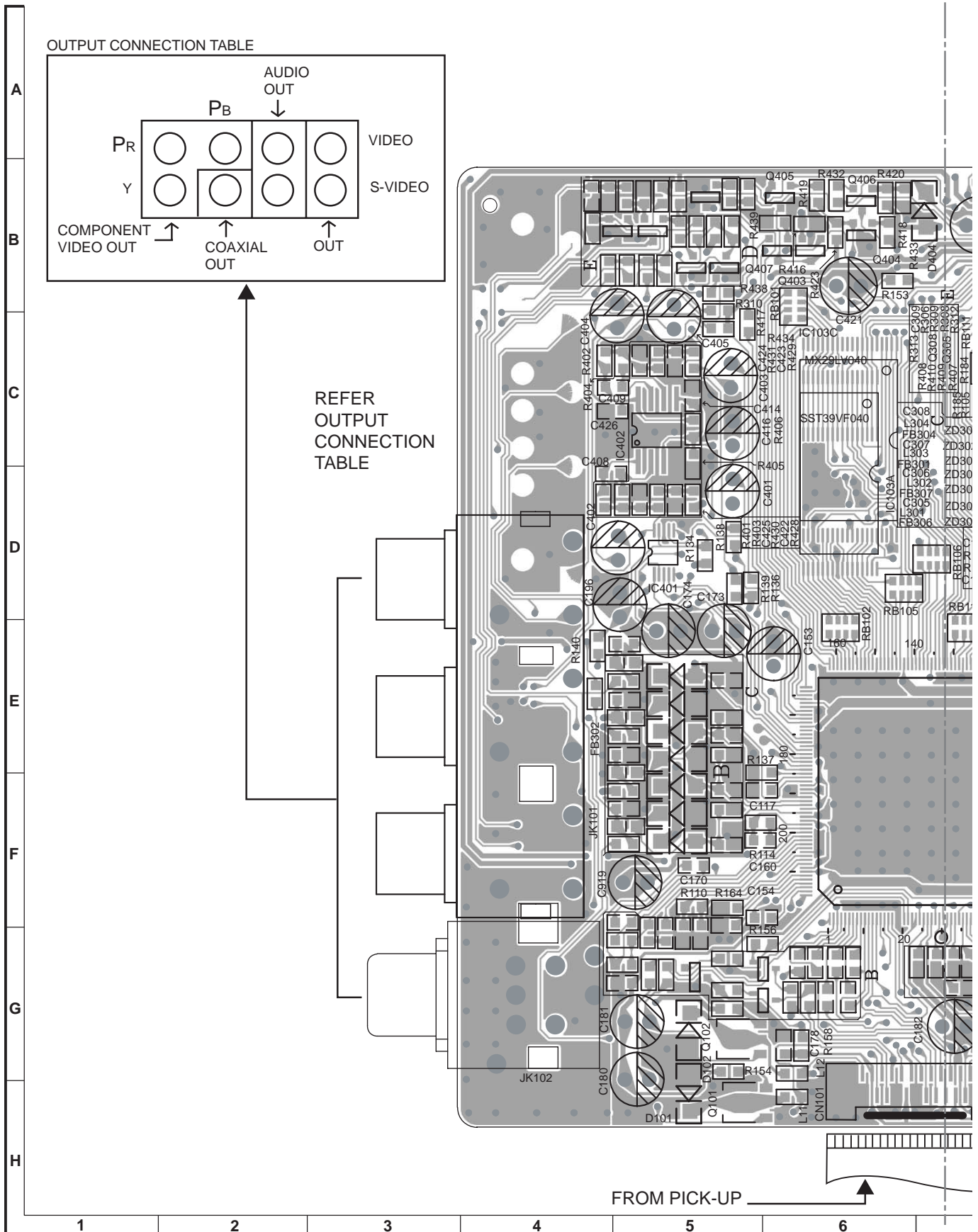


Figure 2: WIRING SIDE OF MAIN PCB (TOP VIEW) (1/2)

WIRING SIDE OF MAIN PCB (TOP VIEW)

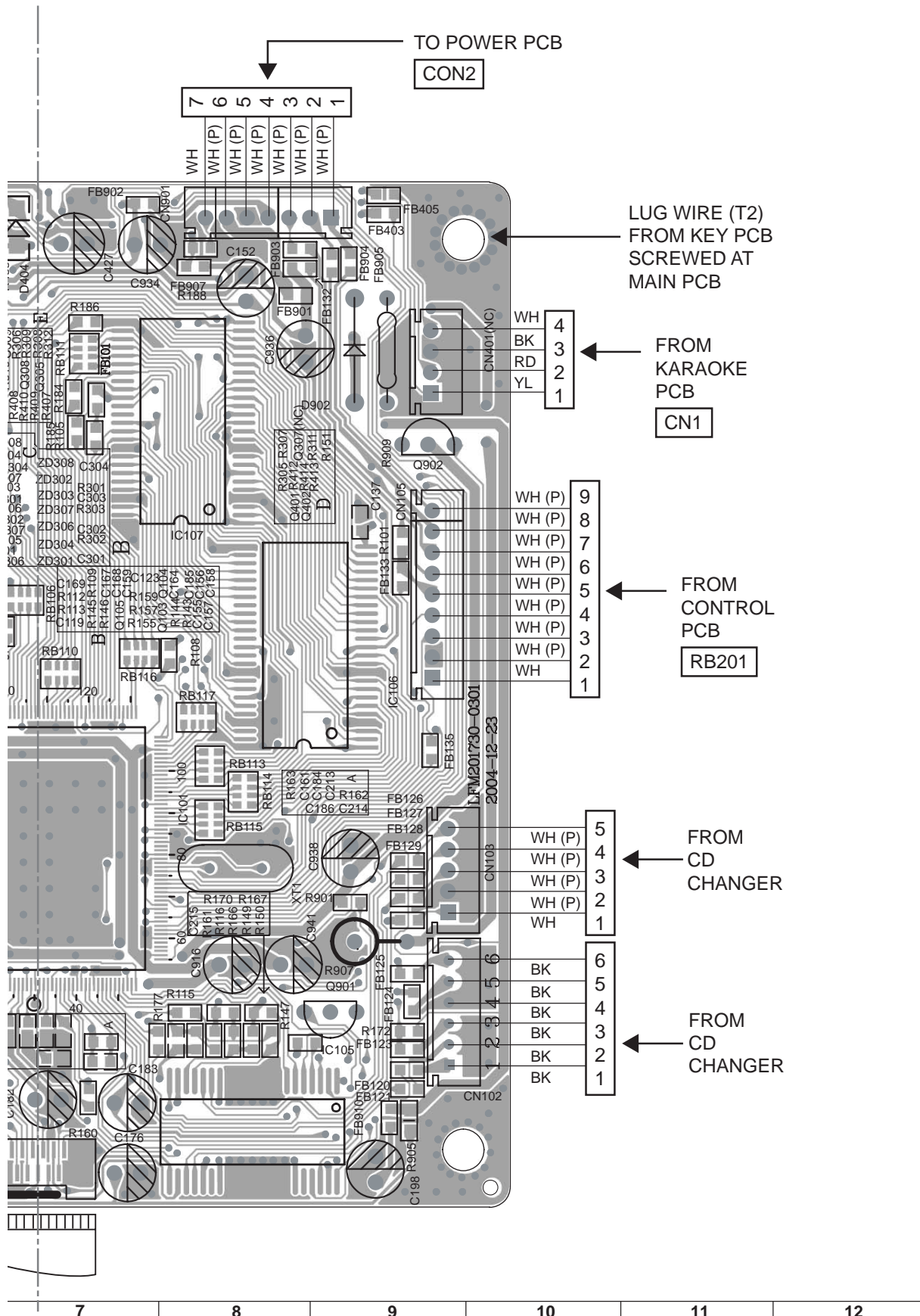


Figure 2: WIRING SIDE OF MAIN PCB (TOP VIEW) (2/2)

WIRING SIDE OF MAIN PCB (BOTTOM VIEW)

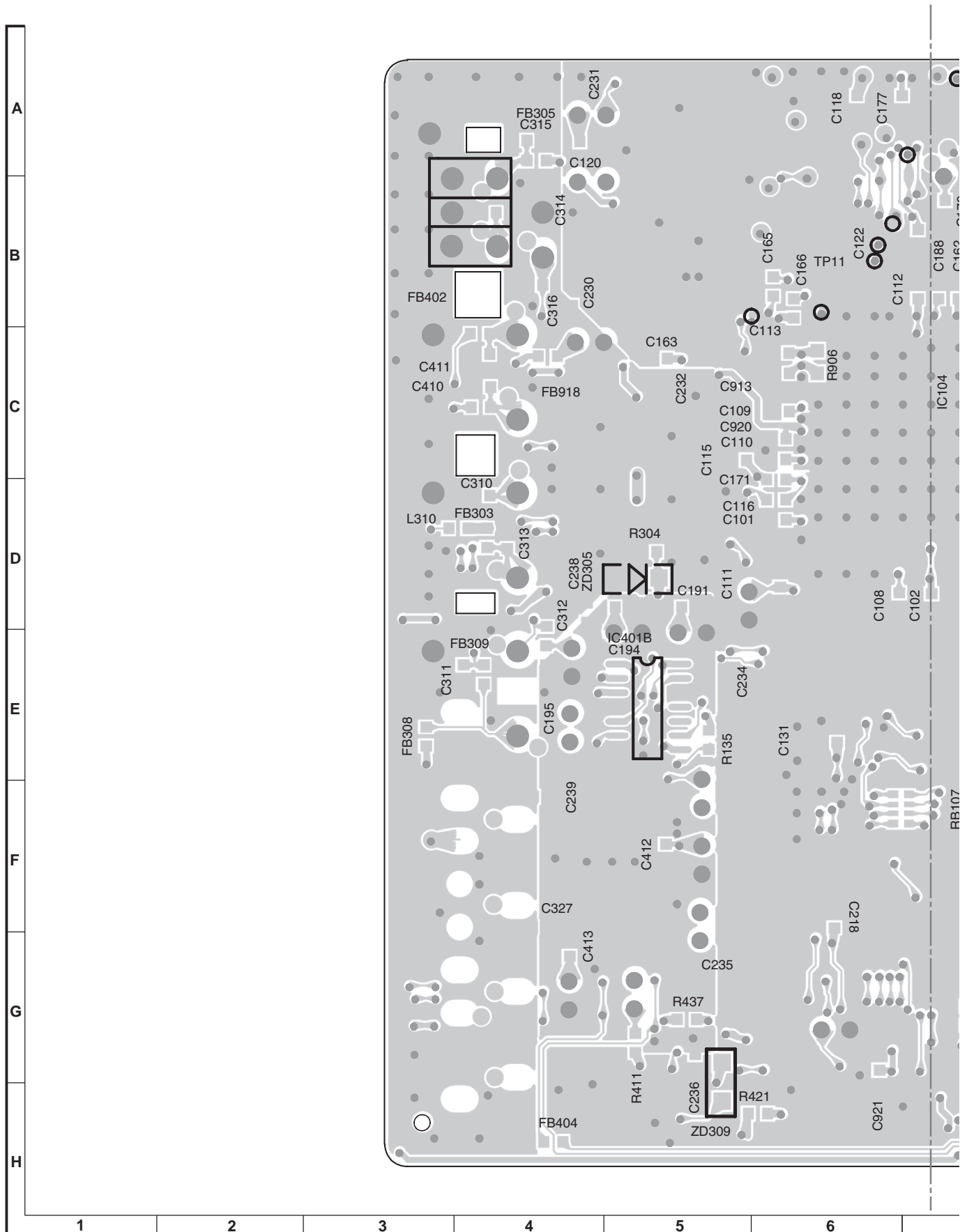


Figure 3: WIRING SIDE OF MAIN PCB (BOTTOM VIEW) (1/2)

WIRING SIDE OF MAIN PCB (BOTTOM VIEW)

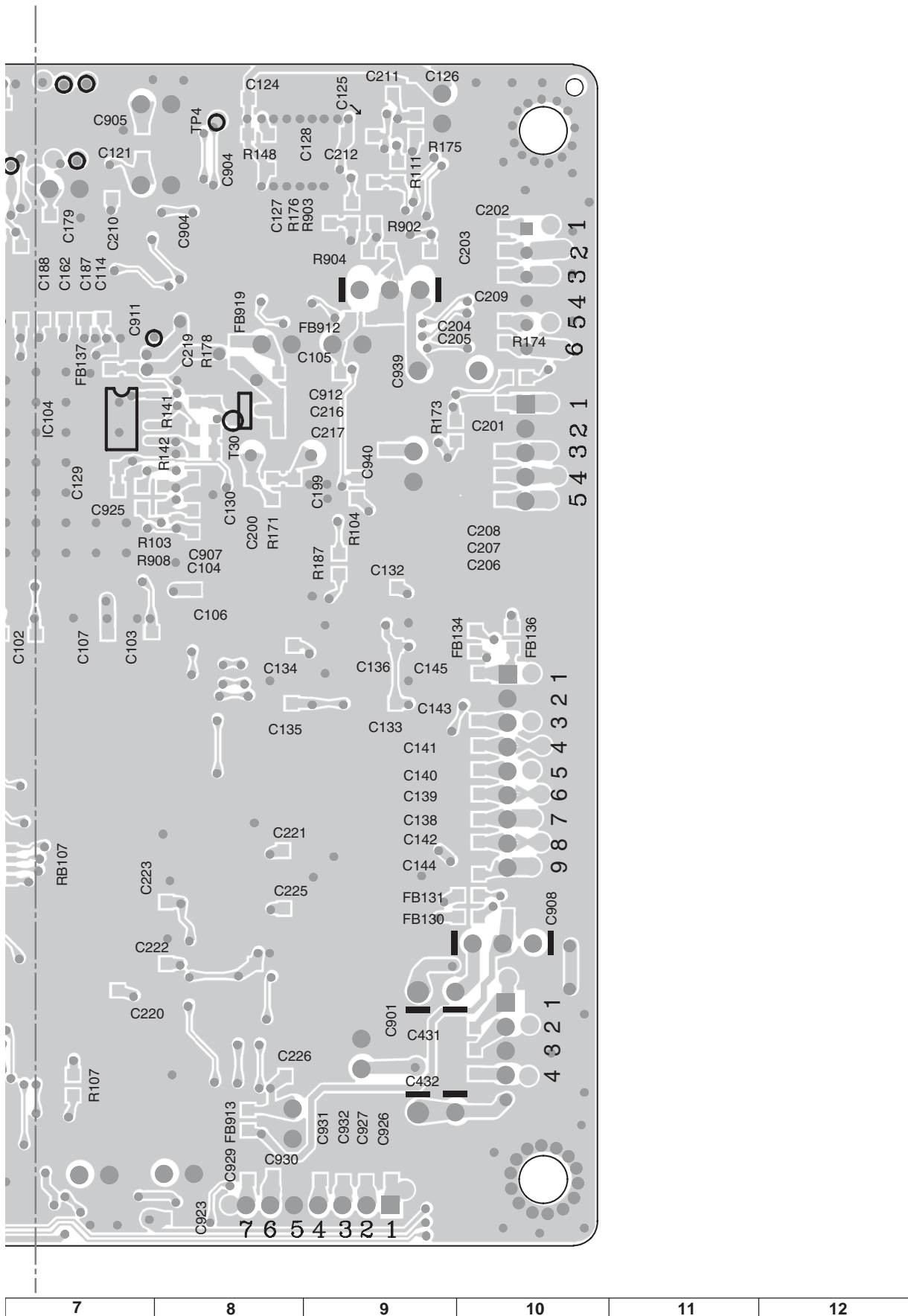


Figure 3: WIRING SIDE OF MAIN PCB (BOTTOM VIEW) (2/2)

WIRING SIDE OF KEY PCB (TOP VIEW)

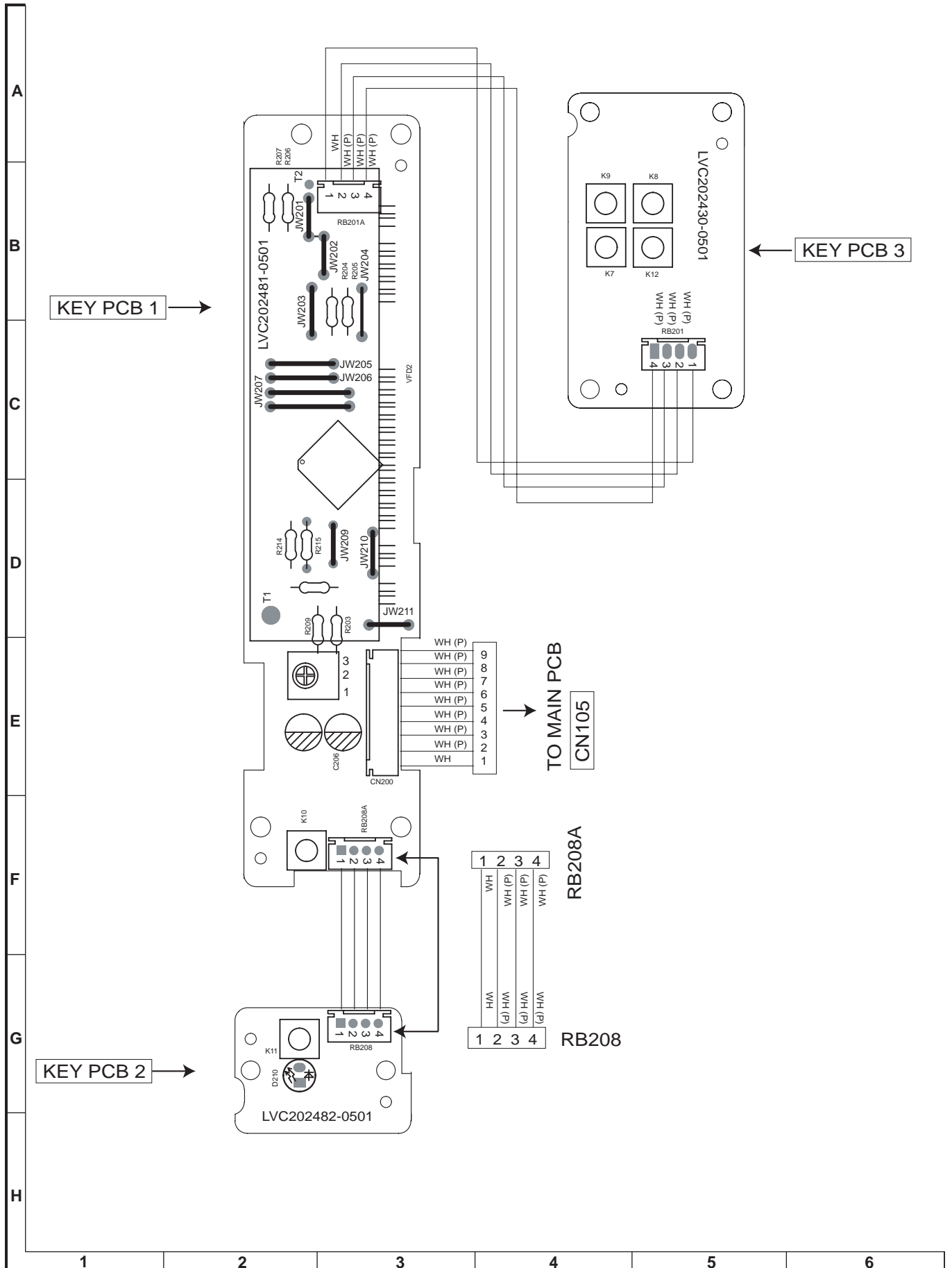


Figure 4: WIRING SIDE OF KEY PCB (TOP VIEW)

WIRING SIDE OF KEY PCB (BOTTOM VIEW)

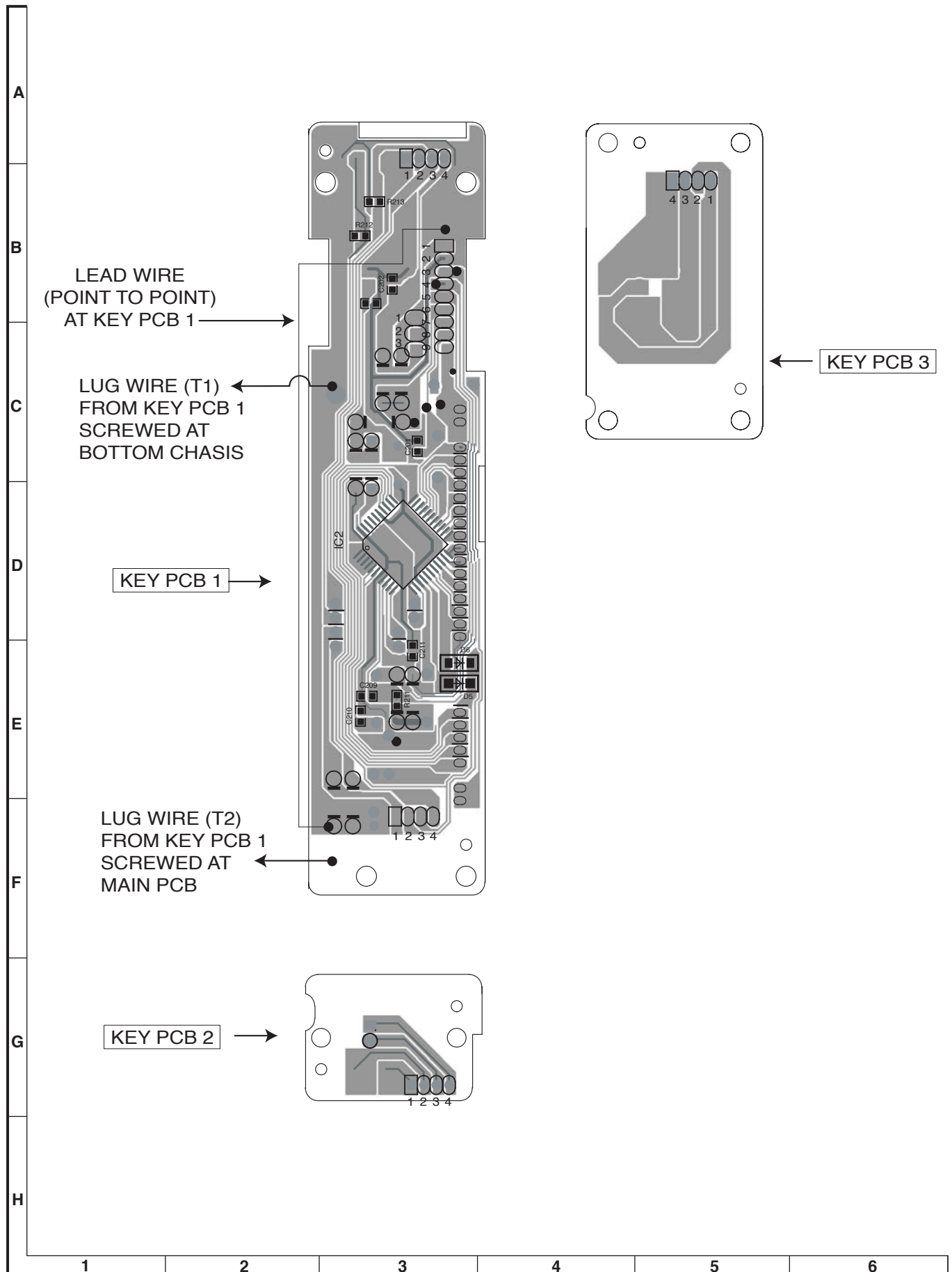


Figure 4: WIRING SIDE OF KEY PCB (BOTTOM VIEW)

WIRING SIDE OF KARAOKE PCB (TOP VIEW)

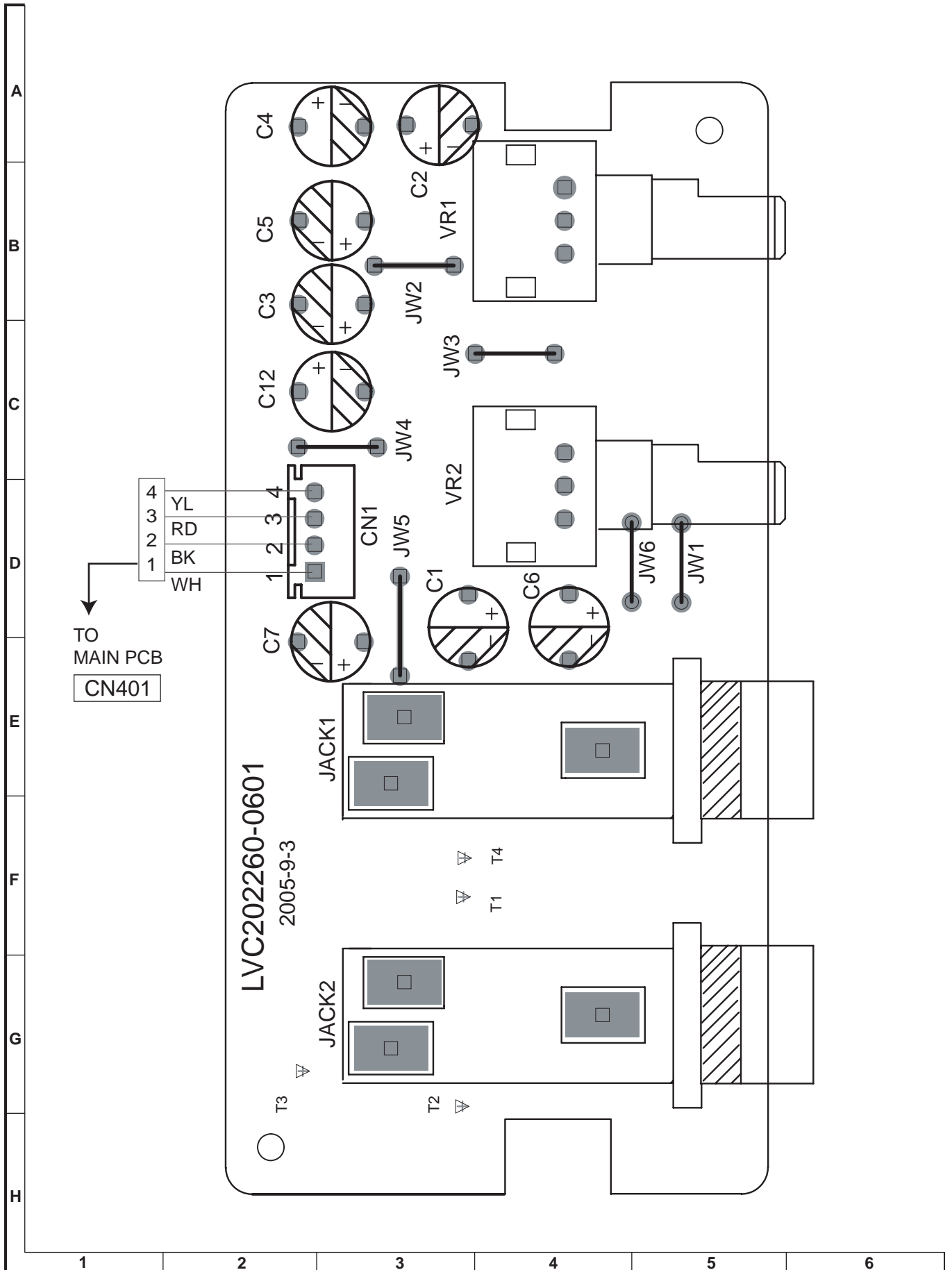


Figure 5: WIRING SIDE OF KARAOKE PCB (TOP VIEW)

WIRING SIDE OF KARAOKE PCB (BOTTOM VIEW)

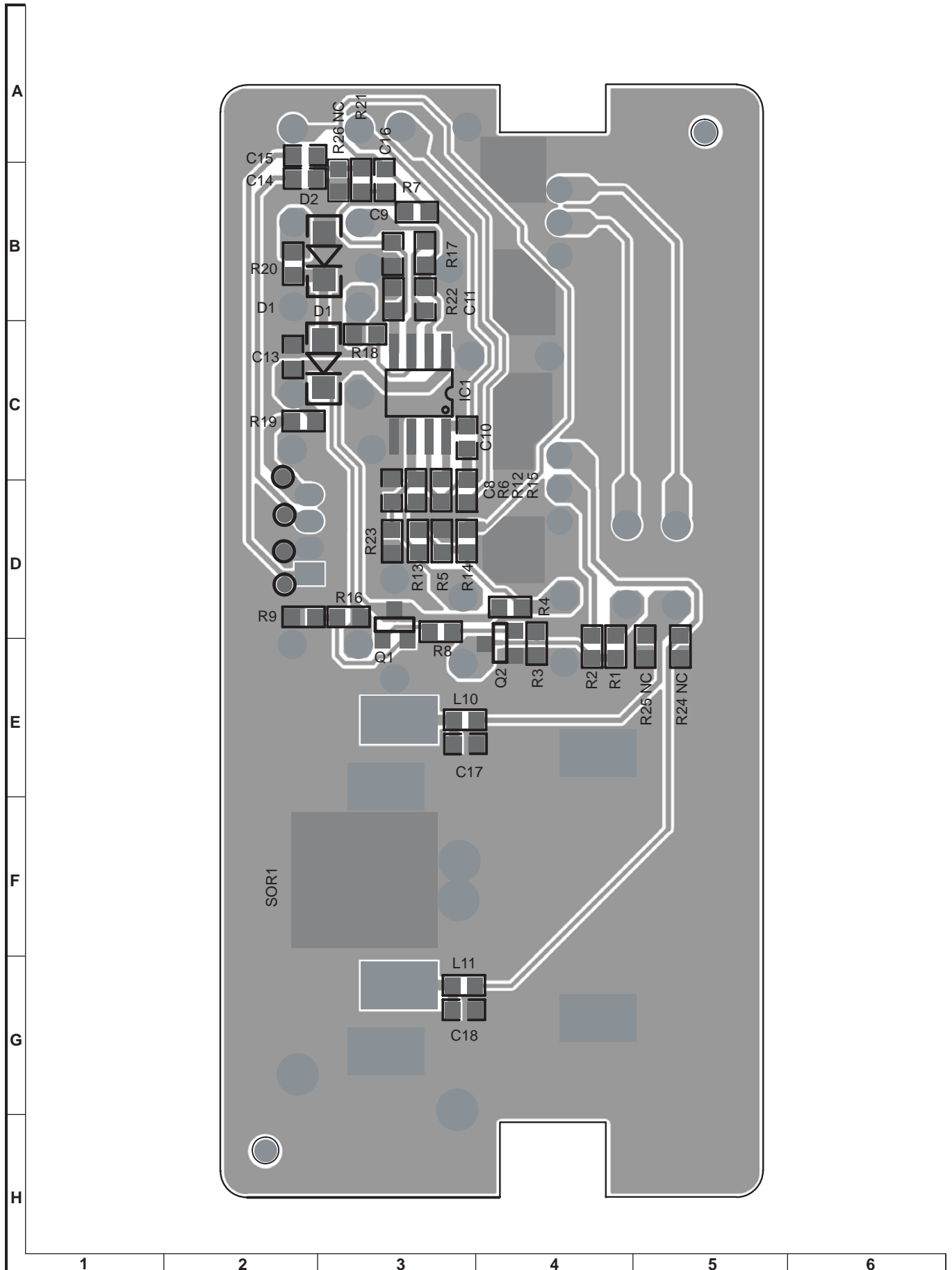


Figure 5: WIRING SIDE OF KARAOKE PCB (BOTTOM VIEW)

NOTES ON SCHEMATIC DIAGRAM

● Resistor:

To differentiate the units of resistors, such symbol as K and M are used; the symbol K means 1000 ohm and the symbol M means 1000 kohm and the resistor without any symbol is ohm-type resistor. Besides, the one with “Fusible” is a fuse type.

● Capacitor:

To indicate the unit of capacitor, a symbol P is used: this symbol P means pico-fared and the unit of the capacitor without such a symbol is microfared. As to electrolytic capacitor, the expression “capacitance/withstand voltage” is used.

(CH), (TH), (RH), (UJ): Temperature compensation

(ML): Mylar type

(P.P.): Polypropylene type

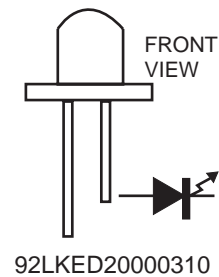
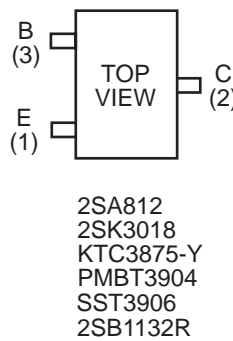
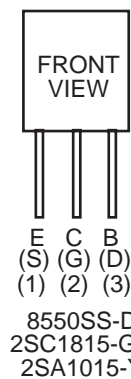
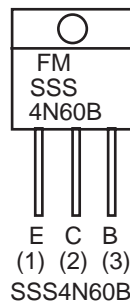
● Schematic diagram and Wiring Side of P.W. Board for this model are subject to change for improvement without prior notice.

● The indicated voltage in each section is the one measured by Digital Multimeter between such a section and the chassis with no signal given.

● Parts marked with “△ (□=□=□) are are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

REF. No.	DESCRIPTION	POSITION
K7	PLAY	ON-OFF
K8	FAST FORWARD	ON-OFF
K9	STOP	ON-OFF
K10	EJECT	ON-OFF
K11	ON/STANDBY	ON-OFF
K12	REVERSE	ON-OFF
VR1	MIC VOLUME	MAX-MIN
VR2	MIC VOLUME	MAX-MIN

TYPES OF TRANSISTOR AND LED



TROUBLESHOOTING

If you experience any of the following difficulties while using the system, use troubleshooting guide to help you remedy the problem. Should any problem persist, consult your nearest service center.

No power:

- Is the power cord firmly plugged into the power outlet?
- One of the safety mechanisms may be operating. In this event, unplug the player from the power outlet briefly and then plug it in again.

No picture:

- Check that the system is connected securely.
- The video connecting system cord is damaged. Replace it with a new one.
- Make sure you connect the system to video input connector on the TV.
- Make sure you turn on the TV.
- Make sure you select the video input on the TV so that you can view the pictures from this system.

The picture noise appears:

- Clear the disc.
- If video from this system has to go through your VCR to get to your TV, the copy-protection applied to some DVD programs could affect picture quality. If you still experience problems after checking your connections, please try connecting your DVD system directly to your TV's S-Video input, if your TV is equipped with this input.

The aspect ratio of the screen cannot be changed even though you set "TV DISPLAY" in the SETUP menu when you play a wide picture:

- The aspect rate is fixed on your DVD disc.
- If you connect the system with the S-Video cable, connect directly to the TV. Otherwise, you may not change the aspect rate.
- Depending on the TV, you may not change the aspect rate.

There is no sound or only a very low-level sound is heard:

- Check that the speakers and components are connected securely.
- Make sure that you have selected the correct source on the system.
- The protective device on the system has been activated because of a short circuit. Turn off the system, eliminate the short-circuit problem and turn on the power again.
- The audio connecting cord is damaged. Replace it with a new one.
- The system or fast reverse is performed. Press PLAY/PAUSE ►/■ to return to normal play mode.
- Check the speaker settings.

The left and right sounds are unbalanced or reversed:

- Check that the speakers and components are connected correctly and securely.
- Adjust front balance parameter using SELECT and VOLUME +/-.

Severe hum or noise is heard:

- Check that the speakers and components are connected correctly and securely.
- Check that the connecting cords are away from a transformer or motor, and at least 3 meters away from a TV set or fluorescent light.
- Move your TV away from the audio components.
- The plugs and jacks are dirty, wipe them with a cloth slightly moistened with alcohol.
- Clear the disc.

The sound losses stereo effect when you play a Video CD or a CD:

- Set the Audio mode to "STEREO" in the SETUP menu.
- Make sure you connect the system appropriately.
- The surround effect is difficult to hear when you are playing a Dolby Digital sound track.
- Check the speaker connections.
- Depending on the DVD disc, the output signal may not be the entire 5.1 channel but monaural or stereo even if the sound track is recorded in Dolby Digital format.

The sound comes from the center speaker only:

- Depending on the disc, the sound may come from the center speaker only.

No sound is heard from the center speaker:

- Make sure the Center is set to "ON" in SETUP menu.
- You may set the listening mode to Dolby Pro Logic Phantom.
- Adjust the speaker volume.

No sound or only a very low-level sound is heard from the rear speakers:

- Make sure the rear is set to "ON" in SETUP menu.
- Adjust the speaker volume.

The language for the subtitles cannot be changed when you play a DVD:

- Multilingual subtitles are not recorded on the DVD.
- Changing the language for the subtitles is prohibited on the DVD.

The subtitles cannot turn off when you play a DVD:

- Depending on the DVD, you may not be able to turn the subtitles off.

The angles cannot be changed when you play a DVD:

- Multi-angles are not recorded on the DVD.
- Change the angles when the angle mark appears on the TV screen.
- Changing the angles is prohibited on the DVD.

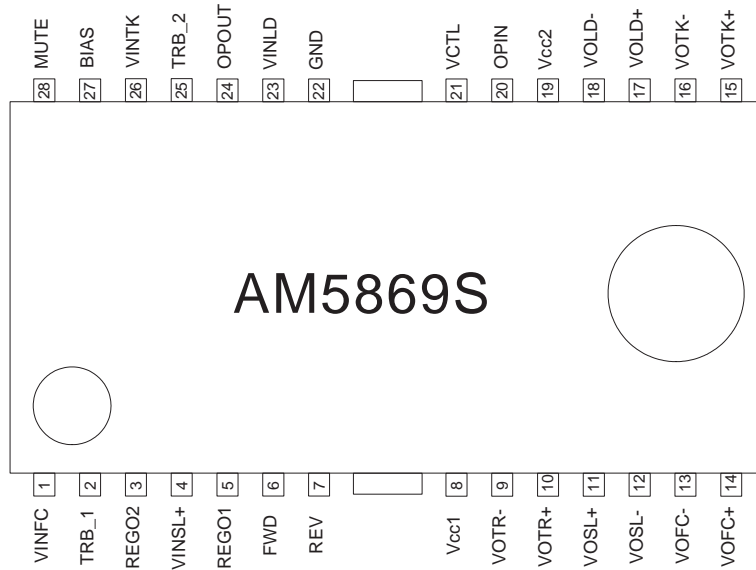
The system does not operate properly:

- Static electricity, etc., may affect the system's operation.
- Press the POWER button to turn off, then press again to turn on.

IC PIN FUNCTION DESCRIPTIONS

IC105 5 Channel BTL Driver for DVD PLayer

Pin Configuration:



Pin Description:

Pin(S)	Name	Description
PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	TRB_1	connect to external transistor base
3	REGO2	Regulator voltage output, connect to external transistor collector
4	VINSL+	Input for the sled driver
5	REGO1	Regulator voltage output, connect to external transistor collector
6	FWD	Tray driver forward input
7	REV	Tray driver reverse input
8	Vcc1	Vcc for pre-drive block and power block of sled and tray
9	VOTR-	Tray driver output(-)
10	VOTR+	Tray driver output(+)
11	VOSL+	Sled driver output(+)
12	VOSL-	Sled driver output(-)
13	VOFC-	Focus driver output(-)
14	VOFC+	Focus driver output(+)
15	VOTK+	Tracking driver output(+)
16	VOTK-	Tracking driver output(-)
17	VOLD+	Spindle driver output(+)
18	VOLD-	Spindle driver output(-)
19	Vcc2	Vcc for power block of spindle, tracking and focus
20	OPIN	Comparator input
21	VCTL	Speed control input of tray driver
22	GND	Ground
23	VINLD	Input for spindle driver
24	OPOUT	Comparator output
25	TRB_2	Connect to external transistor base
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	MUTE	Input for mute control

NOTES) Symbol of +and- (output of drivers) means polarity to input pin.

(For example, if voltage of pin1 is high, pin14 is high.)

IC105 5 Channel BTL Driver for DVD PLayer

Tray driver logic input:

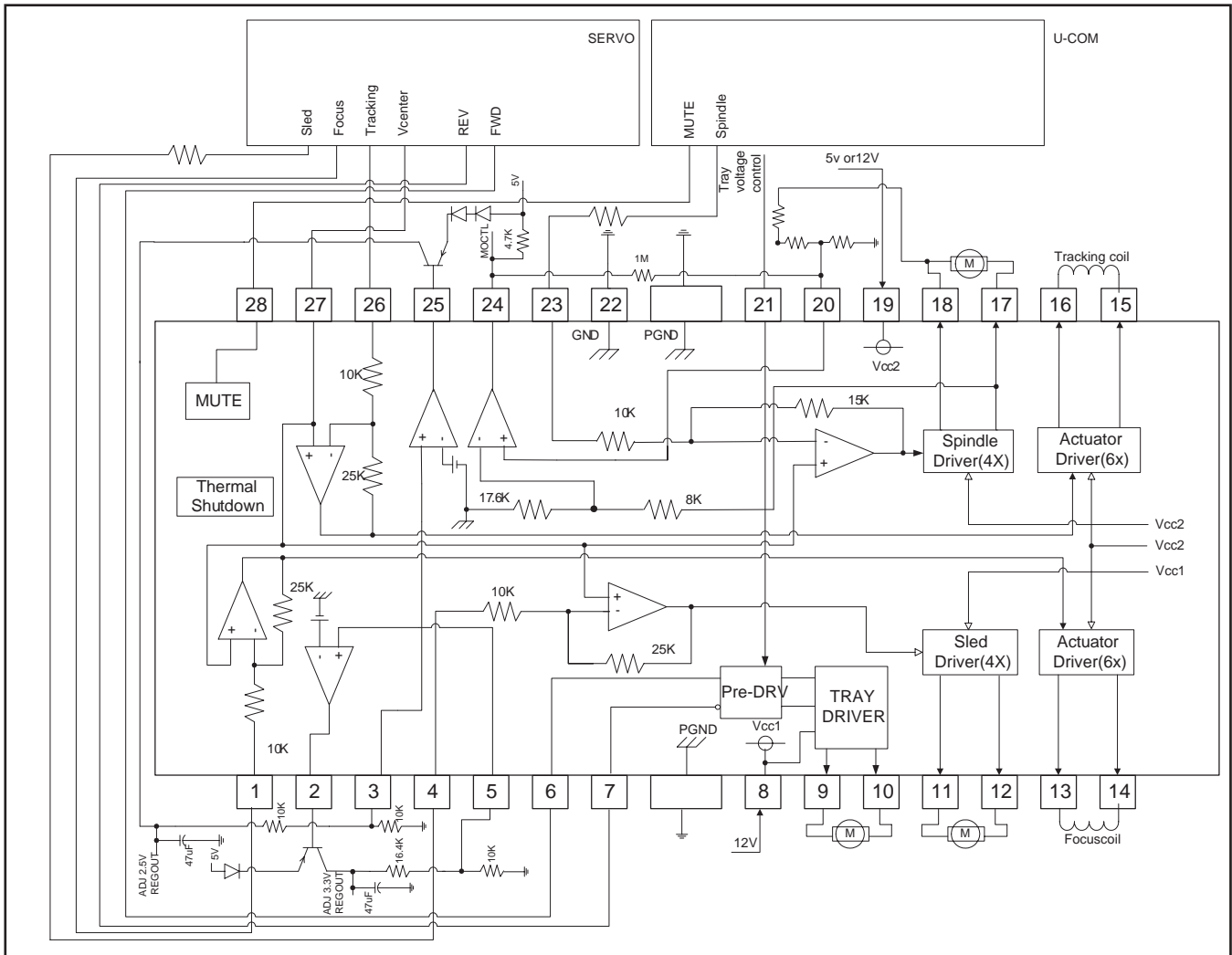
FWD(pin6)	REV(pin7)	VOTR+(pin10)	VOTR-(pin9)	Function
L	L	OPEN	OPEN	Open mode
L	H	L	H	Reverse mode
H	L	H	L	Forward mode
H	H	L	L	Brake mode

Input circuit of pin6 and pin7 is designed to avoid simultaneous activation of upper and lower output tr.; however, in order to improve reliability, apply motor forward/reverse input once through open mode.

We recommend time period for open longer than 10msec.

“H” side Output voltage on output voltage (VOL+, VOL-) varies depending on output control terminal for tray (pin21). “H” side output voltage is set three times (9.2dB Typ)VTCL(pin21). And, “L” side output voltage is equal to output saturation voltage.

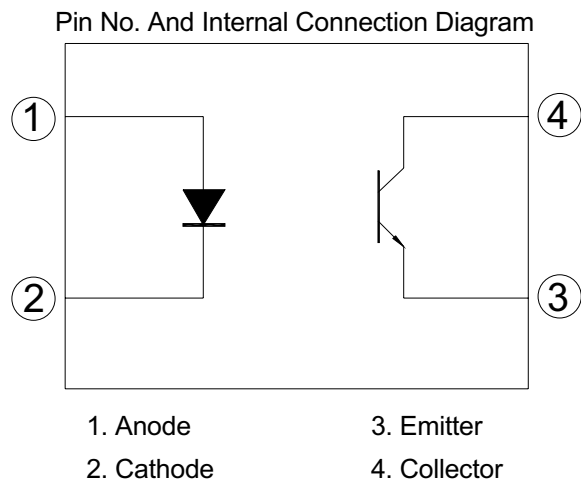
Application circuit:



DV-SL800W

PC1, Optical Sensor (EL-817)

Pin Configuration:



U1, Voltage Regulator (TL431)

Pin Configuration:

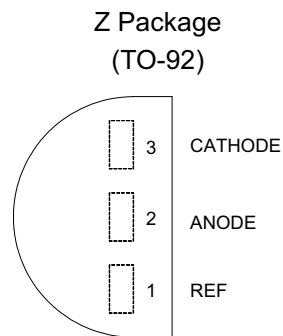


Figure 1: PIN CONFIGURATION OF TL431

Functional Block Diagram:

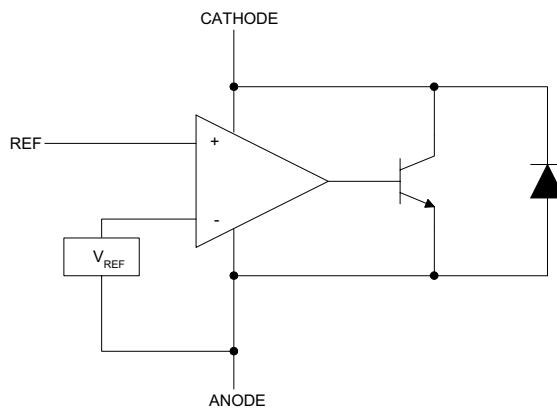
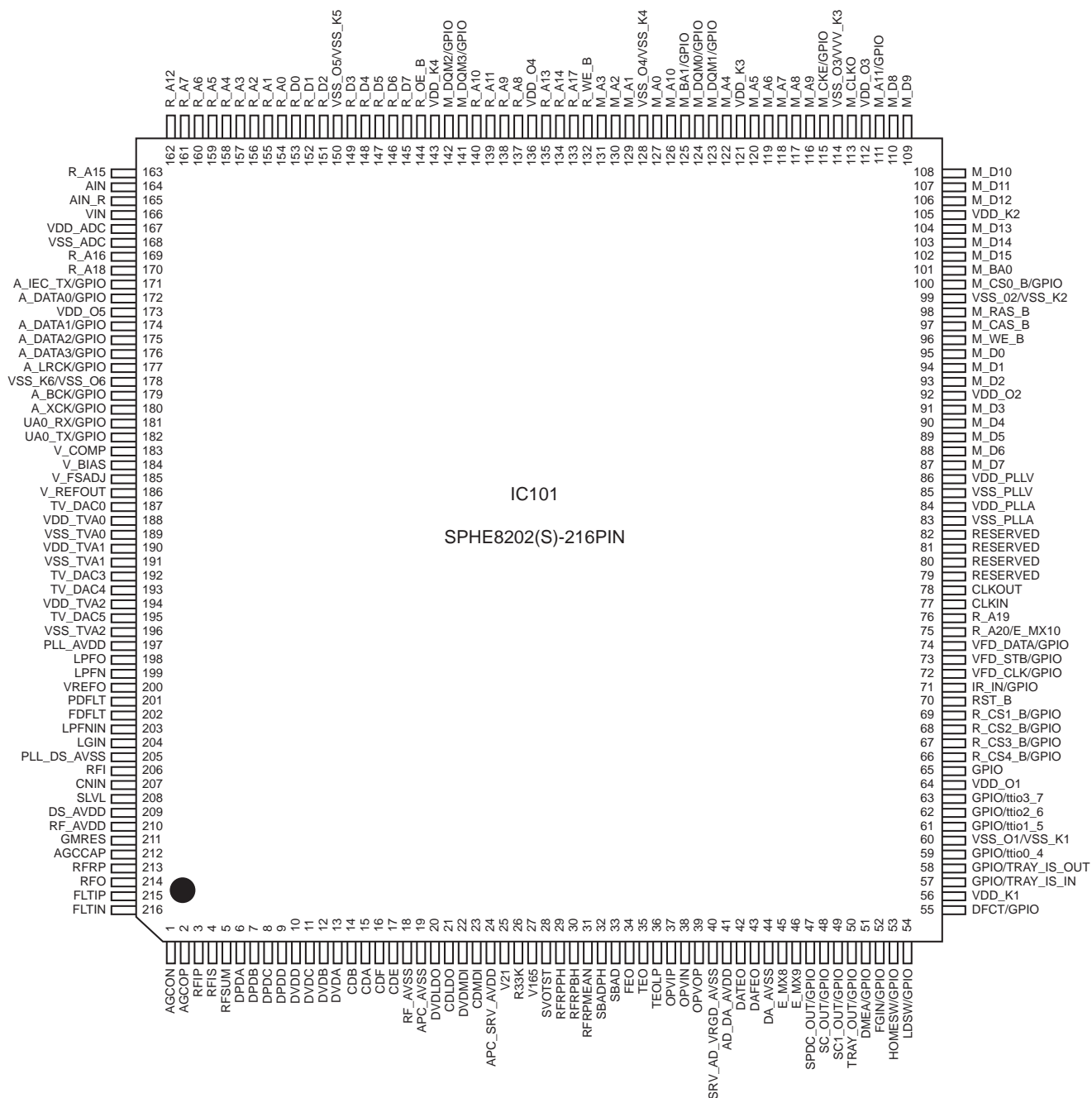


Figure 2: FUNCTIONAL BLOCK DIAGRAM OF TL431

IC101, DVD SINGLE CHIP MPEG A/V PROCESSOR

Pin Configuration:



DV-SL800W
Pin Group Map

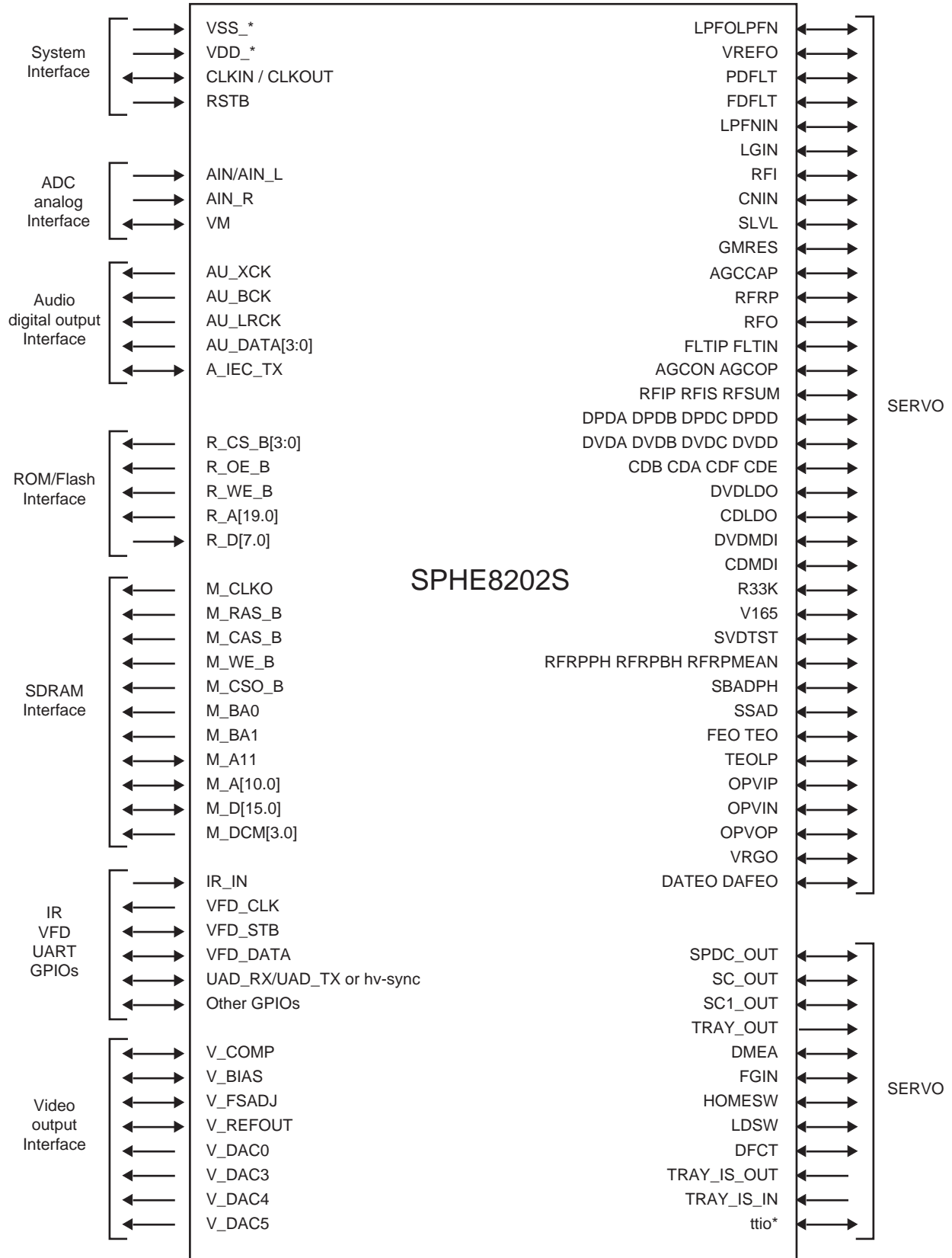


Table 1 ES6629 Pin Description

Name	Pin No	I/O	Definition
AGCON	1	O	Differential AGC output #N
AGCOP	2	O	Differential AGC output #P
RFIP	3	I	Differential RF input #P
RFIS	4	I	Single-ended RF equalizer input.
RFSUM	5	O	RF summing amplified output.
DPDA	6	I	AC coupled RF inputs for the DPD #A, from the main beam photo detector.
DPDB	7	I	AC coupled RF inputs for the DPD #B, from the main beam photo detector.
DPDC	8	I	AC coupled RF inputs for the DPD #C, from the main beam photo detector.
DPDD	9	I	AC coupled RF inputs for the DPD #D, from the main beam photo detector.
DVDD	10	I	DVD RF inputs #A, from the main beam photo detector.
DVDC	11	I	DVD RF inputs #B, from the main beam photo detector.
DVDB	12	I	DVD RF inputs #C, from the main beam photo detector.
DVDA	13	I	DVD RF inputs #D, from the main beam photo detector.
CDB	14	I	CD RF inputs #B, from the main beam photo detector.
CDA	15	I	CD RF inputs #A, from the main beam photo detector.
CDF	16	I	CD tracking error inputs #F, from the main beam photo detector.
CDE	17	I	CD tracking error inputs #E, from the main beam photo detector.
RF_AVSS	18	S	Servo RF ground.
APC_AVSS	19	S	Servo APC ground.
DVDLDO	20	O	DVD APC output.
CDLDO	21	O	CD APC output.
DVMDI	22	I	DVD APC input from monitor photo diode.
CDMDI	23	I	CD APC input from monitor photo diode.
APC_SRV_AVDD	24	S	Servo PC and analog 3.3V power (216pin only)
V21	25	-	Reference DC bias voltage.
R33K	26	-	External reference resistor input.
V165	27	-	Reference DC bias voltage.
SVOTST	28	O	RF peak hold external capacitor.
RFRPPH	29	O	RFRP peak hold signal output.
RFRPBH	30	O	RFRP bottom hold signal output.
RFRMEAN	31	O	RFRP mean signal output.
SBADPH	32	O	Sub-beam adds peak hold signal output.
SBAD	33	O	Sub-beam adds signal output.
FEO	34	O	Focus error signal output.
TEO	35	O	Tracking error signal output.
TEOLP	36	A	
OPVIP	37	I	Op-amp 1 positive input.
OPVIN	38	I	Op-amp 1 negative input.
OPVOP	39	O	Op-amp output.
SRV_AD_VRGD_AVSS	40	S	Servo/ADC analog ground
AD_DA_AVDD	41	S	Servo ADC/DAC 3.3V power
DATEO	42	A	
DAFEO	43	A	
DA_AVSS	44	S	Servo DAC ground

Symbol	Pin NO	I/O	Description																								
E_MXS	45	I/O	GPIO[70]																								
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[5:4]=2'b01</td> <td>UA1_RXD</td> <td>I</td> </tr> <tr> <td>sft_cfg7[5:4]=2'b11</td> <td>656_DATA[0]</td> <td>O</td> </tr> <tr> <td>sft_cfg1[11:9]=3'b110</td> <td>RISC_INT1_11</td> <td>I</td> </tr> <tr> <td>sft_cfg7[11]=1'b0, sft_cfg0[11]=1'b1, fm_qpio_len[3:0]>8</td> <td>FM_GPICB[12]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg0[11]=1'b0, fm_qpio_len[3:0]4'b1100</td> <td>FM_GPICB[29]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[5]=1'b1</td> <td>TV_EXT_DATA_Cr[7]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[70](default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[5:4]=2'b01	UA1_RXD	I	sft_cfg7[5:4]=2'b11	656_DATA[0]	O	sft_cfg1[11:9]=3'b110	RISC_INT1_11	I	sft_cfg7[11]=1'b0, sft_cfg0[11]=1'b1, fm_qpio_len[3:0]>8	FM_GPICB[12]	I/O	sft_cfg0[11]=1'b0, fm_qpio_len[3:0]4'b1100	FM_GPICB[29]	I/O	sft_cfg8[5]=1'b1	TV_EXT_DATA_Cr[7]	I	(other)	GPIO[70](default)	I/O
			Priority selection	Function	Dir																						
			sft_cfg2[5:4]=2'b01	UA1_RXD	I																						
			sft_cfg7[5:4]=2'b11	656_DATA[0]	O																						
			sft_cfg1[11:9]=3'b110	RISC_INT1_11	I																						
			sft_cfg7[11]=1'b0, sft_cfg0[11]=1'b1, fm_qpio_len[3:0]>8	FM_GPICB[12]	I/O																						
			sft_cfg0[11]=1'b0, fm_qpio_len[3:0]4'b1100	FM_GPICB[29]	I/O																						
sft_cfg8[5]=1'b1	TV_EXT_DATA_Cr[7]	I																									
(other)	GPIO[70](default)	I/O																									
E_MXS	46	I/O	GPIO[71]																								
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[5:4]=2'b01</td> <td>UA1_TXD</td> <td>O</td> </tr> <tr> <td>sft_cfg7[5:4]=2'b11</td> <td>656_DATA[1]</td> <td>O</td> </tr> <tr> <td>sft_cfg1[11:9]=3'b110</td> <td>RISC_INT1_12</td> <td>I</td> </tr> <tr> <td>sft_cfg7[11]=1'b0, sft_cfg0[11]=1'b1, fm_qpio_len[3:0]>8</td> <td>FM_GPIOB[13]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg0[11]=1'b 0, fm_qpio_len[3:0]4'b1100</td> <td>FM_GPICB[30]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[5]=1'b1</td> <td>TV_EXT_DATA_Cr[6]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[71](default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[5:4]=2'b01	UA1_TXD	O	sft_cfg7[5:4]=2'b11	656_DATA[1]	O	sft_cfg1[11:9]=3'b110	RISC_INT1_12	I	sft_cfg7[11]=1'b0, sft_cfg0[11]=1'b1, fm_qpio_len[3:0]>8	FM_GPIOB[13]	I/O	sft_cfg0[11]=1'b 0, fm_qpio_len[3:0]4'b1100	FM_GPICB[30]	I/O	sft_cfg8[5]=1'b1	TV_EXT_DATA_Cr[6]	I	(other)	GPIO[71](default)	I/O
			Priority selection	Function	Dir																						
			sft_cfg2[5:4]=2'b01	UA1_TXD	O																						
			sft_cfg7[5:4]=2'b11	656_DATA[1]	O																						
			sft_cfg1[11:9]=3'b110	RISC_INT1_12	I																						
			sft_cfg7[11]=1'b0, sft_cfg0[11]=1'b1, fm_qpio_len[3:0]>8	FM_GPIOB[13]	I/O																						
			sft_cfg0[11]=1'b 0, fm_qpio_len[3:0]4'b1100	FM_GPICB[30]	I/O																						
sft_cfg8[5]=1'b1	TV_EXT_DATA_Cr[6]	I																									
(other)	GPIO[71](default)	I/O																									
SPDC_OUT/GPIO	47	I/O	Servo SPDC_OUT																								
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_RESET_B</td> <td>O</td> </tr> <tr> <td>sft_cfg4[0]=1'b1</td> <td>SPDC_OUT (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDF</td> <td>I</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_ADDR[0]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[0]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_RESET_B	O	sft_cfg4[0]=1'b1	SPDC_OUT (default)	I/O	sft_cfg8[9]=1'b1	DAC_PDF	I	sft_cfg8[8]=1'b1	OTP_TEST_ADDR[0]	I	(other)	GPIO[0]	I/O						
			Priority selection	Function	Dir																						
			sft_cfg2[11:10]=2'b01,2'b10	AT_RESET_B	O																						
			sft_cfg4[0]=1'b1	SPDC_OUT (default)	I/O																						
			sft_cfg8[9]=1'b1	DAC_PDF	I																						
			sft_cfg8[8]=1'b1	OTP_TEST_ADDR[0]	I																						
(other)	GPIO[0]	I/O																									
SC_OUT/GPIO	48	I/O	Servo SC_OUT																								
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_DIOR_B</td> <td>O</td> </tr> <tr> <td>sft_cfg4[1]=1'b1</td> <td>SC_OUT (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDE</td> <td>I</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_ADDR[1]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[1]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_DIOR_B	O	sft_cfg4[1]=1'b1	SC_OUT (default)	I/O	sft_cfg8[9]=1'b1	DAC_PDE	I	sft_cfg8[8]=1'b1	OTP_TEST_ADDR[1]	I	(other)	GPIO[1]	I/O						
			Priority selection	Function	Dir																						
			sft_cfg2[11:10]=2'b01,2'b10	AT_DIOR_B	O																						
			sft_cfg4[1]=1'b1	SC_OUT (default)	I/O																						
			sft_cfg8[9]=1'b1	DAC_PDE	I																						
sft_cfg8[8]=1'b1	OTP_TEST_ADDR[1]	I																									
(other)	GPIO[1]	I/O																									
SC1_OUT/GPIO	49	I/O	Servo SC1_OUT																								
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_DIOW_B</td> <td>O</td> </tr> <tr> <td>sft_cfg4[2]=1'b1</td> <td>SC1_OUT (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDD</td> <td>I</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_ADDR[2]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[2]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_DIOW_B	O	sft_cfg4[2]=1'b1	SC1_OUT (default)	I/O	sft_cfg8[9]=1'b1	DAC_PDD	I	sft_cfg8[8]=1'b1	OTP_TEST_ADDR[2]	I	(other)	GPIO[2]	I/O						
			Priority selection	Function	Dir																						
			sft_cfg2[11:10]=2'b01,2'b10	AT_DIOW_B	O																						
			sft_cfg4[2]=1'b1	SC1_OUT (default)	I/O																						
			sft_cfg8[9]=1'b1	DAC_PDD	I																						
sft_cfg8[8]=1'b1	OTP_TEST_ADDR[2]	I																									
(other)	GPIO[2]	I/O																									

Symbol	Pin NO	I/O	Description																														
TRAY_OUT/GPIO	50	I/O	Servo TRAY_OUT <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_IORDY</td> <td>I</td> </tr> <tr> <td>sft_cfg4[3]=1'b1</td> <td>TRAY_OUT (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDC</td> <td>I</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_ADDR[3]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[3]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_IORDY	I	sft_cfg4[3]=1'b1	TRAY_OUT (default)	I/O	sft_cfg8[9]=1'b1	DAC_PDC	I	sft_cfg8[8]=1'b1	OTP_TEST_ADDR[3]	I	(other)	GPIO[3]	I/O												
Priority selection	Function	Dir																															
sft_cfg2[11:10]=2'b01,2'b10	AT_IORDY	I																															
sft_cfg4[3]=1'b1	TRAY_OUT (default)	I/O																															
sft_cfg8[9]=1'b1	DAC_PDC	I																															
sft_cfg8[8]=1'b1	OTP_TEST_ADDR[3]	I																															
(other)	GPIO[3]	I/O																															
DMEA_OUT/GPIO	51	I/O	Servo DMEA <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_DMACK</td> <td>O</td> </tr> <tr> <td>sft_cfg4[4]=1'b1</td> <td>DMEA_OUT (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDB</td> <td>I</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_ADDR[4]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[4]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_DMACK	O	sft_cfg4[4]=1'b1	DMEA_OUT (default)	O	sft_cfg8[9]=1'b1	DAC_PDB	I	sft_cfg8[8]=1'b1	OTP_TEST_ADDR[4]	I	(other)	GPIO[4]	I/O												
Priority selection	Function	Dir																															
sft_cfg2[11:10]=2'b01,2'b10	AT_DMACK	O																															
sft_cfg4[4]=1'b1	DMEA_OUT (default)	O																															
sft_cfg8[9]=1'b1	DAC_PDB	I																															
sft_cfg8[8]=1'b1	OTP_TEST_ADDR[4]	I																															
(other)	GPIO[4]	I/O																															
FGIN/GPIO	52	I/O	Servo FGIN <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_DMARQ</td> <td>I</td> </tr> <tr> <td>sft_cfg4[5]=1'b1</td> <td>FGIN_OUT (default)</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDA</td> <td>I</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_PGM</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[5]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_DMARQ	I	sft_cfg4[5]=1'b1	FGIN_OUT (default)	I	sft_cfg8[9]=1'b1	DAC_PDA	I	sft_cfg8[8]=1'b1	OTP_TEST_PGM	I	(other)	GPIO[5]	I/O												
Priority selection	Function	Dir																															
sft_cfg2[11:10]=2'b01,2'b10	AT_DMARQ	I																															
sft_cfg4[5]=1'b1	FGIN_OUT (default)	I																															
sft_cfg8[9]=1'b1	DAC_PDA	I																															
sft_cfg8[8]=1'b1	OTP_TEST_PGM	I																															
(other)	GPIO[5]	I/O																															
HOMESW/GPIO	53	IO	Servo HOMESW <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[3:2]=2'b10</td> <td>UA0_RXD</td> <td>I</td> </tr> <tr> <td>sft_cfg1[8:6]=3'b010</td> <td>R_CSALL_B</td> <td>O</td> </tr> <tr> <td>sft_cfg7[7:6]=2'b11</td> <td>PCMCIA_IOW_B</td> <td>O</td> </tr> <tr> <td>sft_cfg8[1]=1'b1</td> <td>DSP_FL0</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_F[9]</td> <td>I</td> </tr> <tr> <td>sft_cfg7[14:13]=2'b01</td> <td>EXT_CLK48</td> <td>I</td> </tr> <tr> <td>sft_cfg6[4]=1'b1</td> <td>DELAY_CHAIN1</td> <td>O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>OTP_TEST_DATA</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[6] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[3:2]=2'b10	UA0_RXD	I	sft_cfg1[8:6]=3'b010	R_CSALL_B	O	sft_cfg7[7:6]=2'b11	PCMCIA_IOW_B	O	sft_cfg8[1]=1'b1	DSP_FL0	O	sft_cfg8[9]=1'b1	DAC_DATA_F[9]	I	sft_cfg7[14:13]=2'b01	EXT_CLK48	I	sft_cfg6[4]=1'b1	DELAY_CHAIN1	O	sft_cfg8[8]=1'b1	OTP_TEST_DATA	O	(other)	GPIO[6] (default)	I/O
Priority selection	Function	Dir																															
sft_cfg2[3:2]=2'b10	UA0_RXD	I																															
sft_cfg1[8:6]=3'b010	R_CSALL_B	O																															
sft_cfg7[7:6]=2'b11	PCMCIA_IOW_B	O																															
sft_cfg8[1]=1'b1	DSP_FL0	O																															
sft_cfg8[9]=1'b1	DAC_DATA_F[9]	I																															
sft_cfg7[14:13]=2'b01	EXT_CLK48	I																															
sft_cfg6[4]=1'b1	DELAY_CHAIN1	O																															
sft_cfg8[8]=1'b1	OTP_TEST_DATA	O																															
(other)	GPIO[6] (default)	I/O																															
LDSW/GPIO	54	IO	Servo LDSW <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[3:2]=2'b10</td> <td>UA0_TXD</td> <td>I</td> </tr> <tr> <td>sft_cfg1[8:6]=3'b10</td> <td>UA1_RXD</td> <td>O</td> </tr> <tr> <td>sft_cfg7[7:6]=2'b11</td> <td>PCMCIA_IOR_B</td> <td>O</td> </tr> <tr> <td>sft_cfg8[2]=1'b1</td> <td>DSP_FL1</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_F[8]</td> <td>I</td> </tr> <tr> <td>sft_cfg7[15:14]=2'b11</td> <td>CLK27_OUT</td> <td>I</td> </tr> <tr> <td>sft_cfg7[14:13]=2'b10</td> <td>EXT_CLK48</td> <td>O</td> </tr> <tr> <td>sft_cfg6[4]=1'b1</td> <td>DELAY_CHAIN2</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[7] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[3:2]=2'b10	UA0_TXD	I	sft_cfg1[8:6]=3'b10	UA1_RXD	O	sft_cfg7[7:6]=2'b11	PCMCIA_IOR_B	O	sft_cfg8[2]=1'b1	DSP_FL1	O	sft_cfg8[9]=1'b1	DAC_DATA_F[8]	I	sft_cfg7[15:14]=2'b11	CLK27_OUT	I	sft_cfg7[14:13]=2'b10	EXT_CLK48	O	sft_cfg6[4]=1'b1	DELAY_CHAIN2	O	(other)	GPIO[7] (default)	I/O
Priority selection	Function	Dir																															
sft_cfg2[3:2]=2'b10	UA0_TXD	I																															
sft_cfg1[8:6]=3'b10	UA1_RXD	O																															
sft_cfg7[7:6]=2'b11	PCMCIA_IOR_B	O																															
sft_cfg8[2]=1'b1	DSP_FL1	O																															
sft_cfg8[9]=1'b1	DAC_DATA_F[8]	I																															
sft_cfg7[15:14]=2'b11	CLK27_OUT	I																															
sft_cfg7[14:13]=2'b10	EXT_CLK48	O																															
sft_cfg6[4]=1'b1	DELAY_CHAIN2	O																															
(other)	GPIO[7] (default)	I/O																															

Symbol	Pin NO	I/O	Description		
DFCT/GPIO	55	IO	Servo DFCT		
			Priority selection	Function	Dir
			sft_cfg2[11:10]=2'b01,2'b10	AT_INTRQ	I
			sft_cfg4[6]=1'b1	DFCT (default)	O
			sft_cfg8[8]=1'b1	DAC_DATA_F[7]	I
(other)	GPIO[8]	I/O			
VDD_K1	56	S	Kernel logic power supply #1		
GPIO/TRAY_IS_IN	57	IO	GPIO		
			Priority selection	Function	Dir
			sft_cfg2[11:10]=2'b01,2'b10	AT_ADR[1]	O
			sft_cfg8[3]=1'b1	DSP_FL2	O
			fm_qpio_len[3:0]>0	FM_GPIOB[0]	I/O
			sft_cfg8[9]=1'b1	DAC_DATA_F[6]	I
(other)	GPIO[9] (default)	I/O			
GPIO/TRAY_IS_OUT	58	IO	GPIO		
			Priority selection	Function	Dir
			sft_cfg2[11:10]=2'b01,2'b10	AT_ADR[2]	O
			sft_cfg8[4]=1'b1	DSP_FLAG_OUT	O
			fm_qpio_len[3:0]>0	FM_GPIOB[1]	I/O
			sft_cfg8[9]=1'b1	DAC_DATA_F[5]	I
(other)	GPIO[10] (default)	I/O			
GPIO/ttio0_4	59	IO	GPIO		
			Priority selection	Function	Dir
			sft_cfg2[11:10]=2'b01,2'b10	AT_ADR[0]	O
			sft_cfg4[9]=1'b1	ttio4/ttio0	I/O
			sft_cfg1[11:9]=3'b001	RISC_INT1_11	I
			sft_cfg3[11:10]=2'b01	ADC_BCK, digital audio input interface bit clock	I/O
			fm_qpio_len[3:0]>0	FM_GPIOB[2]	I/O
			sft_cfg8[9]=1'b1	DAC_DATA_F[4]	I
(other)	GPIO[11] (default)	I/O			
VSS_O1/VSS_K1	60	S	Kernel logic power shared ground supply #1		
GPIO/ttio1_5	61	IO	GPIO		
			Priority selection	Function	Dir
			sft_cfg2[11:10]=2'b01,2'b10	AT_CS1	O
			sft_cfg4[9]=1'b1	ttio5/ttio1	I/O
			sft_cfg4[15:13]=3'b001	HSYNC_PC	O
			sft_cfg1[11:9]=3'b001	RISC_INT1_12	I
			sft_cfg3[11:10]=2'b01	ADC_LRCK, digital audio input interface L/R strobe	I/O
			fm_qpio_len[3:0]>0	FM_GPIOB[3]	I/O
			sft_cfg8[9]=1'b1	DAC_DATA_F[3]	I
			(other)	GPIO[12] (default)	I/O

Symbol	Pin NO	I/O	Description																																	
GPIO/ttio2_6	62	IO	GPIO																																	
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[11:10]=2'b01,2'b10</td> <td>AT_CS0</td> <td>O</td> </tr> <tr> <td>sft_cfg4[9]=1'b1</td> <td>ttio6/ttio2</td> <td>I/O</td> </tr> <tr> <td>sft_cfg4[15:13]=3'b001</td> <td>VSYNC_PC</td> <td>O</td> </tr> <tr> <td>sft_cfg3[15:14]=2'b01</td> <td>ISA_IOCHRDY</td> <td>I</td> </tr> <tr> <td>sft_cfg1[11:9]=3'b001</td> <td>RISC_INT1_13</td> <td>I</td> </tr> <tr> <td>sft_cfg3[11:10]=2'b01</td> <td>ADC_DATA, digital audio input interface data</td> <td>I</td> </tr> <tr> <td>fm_qpio_len[3:0]>1</td> <td>FM_GPIOB[4]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_F[2]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[13] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[11:10]=2'b01,2'b10	AT_CS0	O	sft_cfg4[9]=1'b1	ttio6/ttio2	I/O	sft_cfg4[15:13]=3'b001	VSYNC_PC	O	sft_cfg3[15:14]=2'b01	ISA_IOCHRDY	I	sft_cfg1[11:9]=3'b001	RISC_INT1_13	I	sft_cfg3[11:10]=2'b01	ADC_DATA, digital audio input interface data	I	fm_qpio_len[3:0]>1	FM_GPIOB[4]	I/O	sft_cfg8[9]=1'b1	DAC_DATA_F[2]	I	(other)	GPIO[13] (default)	I/O			
			Priority selection	Function	Dir																															
			sft_cfg2[11:10]=2'b01,2'b10	AT_CS0	O																															
			sft_cfg4[9]=1'b1	ttio6/ttio2	I/O																															
			sft_cfg4[15:13]=3'b001	VSYNC_PC	O																															
			sft_cfg3[15:14]=2'b01	ISA_IOCHRDY	I																															
			sft_cfg1[11:9]=3'b001	RISC_INT1_13	I																															
			sft_cfg3[11:10]=2'b01	ADC_DATA, digital audio input interface data	I																															
			fm_qpio_len[3:0]>1	FM_GPIOB[4]	I/O																															
sft_cfg8[9]=1'b1	DAC_DATA_F[2]	I																																		
(other)	GPIO[13] (default)	I/O																																		
GPIO/ttio3_7	63	IO	GPIO																																	
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg4[9]=1'b1</td> <td>ttio7/ttio3</td> <td>I/O</td> </tr> <tr> <td>sft_cfg2[6:8]=2'b11</td> <td>PCMCIA_WAIT_B</td> <td>I</td> </tr> <tr> <td>sft_cfg1[11:8]=4'b0001</td> <td>EXT_CLK27</td> <td>I</td> </tr> <tr> <td>sft_cfg1[11:9]=3'b001</td> <td>RISC_INT1_14</td> <td>I</td> </tr> <tr> <td>fm_qpio_len[3:0]>1</td> <td>FM_GPIOB[5]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_F[0]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[14] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg4[9]=1'b1	ttio7/ttio3	I/O	sft_cfg2[6:8]=2'b11	PCMCIA_WAIT_B	I	sft_cfg1[11:8]=4'b0001	EXT_CLK27	I	sft_cfg1[11:9]=3'b001	RISC_INT1_14	I	fm_qpio_len[3:0]>1	FM_GPIOB[5]	I/O	sft_cfg8[9]=1'b1	DAC_DATA_F[0]	I	(other)	GPIO[14] (default)	I/O									
			Priority selection	Function	Dir																															
			sft_cfg4[9]=1'b1	ttio7/ttio3	I/O																															
			sft_cfg2[6:8]=2'b11	PCMCIA_WAIT_B	I																															
			sft_cfg1[11:8]=4'b0001	EXT_CLK27	I																															
			sft_cfg1[11:9]=3'b001	RISC_INT1_14	I																															
			fm_qpio_len[3:0]>1	FM_GPIOB[5]	I/O																															
sft_cfg8[9]=1'b1	DAC_DATA_F[0]	I																																		
(other)	GPIO[14] (default)	I/O																																		
VDD_O1	64	S	I/O power supply #1																																	
GPIO	65	IO	GPIO																																	
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[5:4]=2'b10</td> <td>UA1_TXD</td> <td>O</td> </tr> <tr> <td>sft_cfg[8:6]=3'b001</td> <td>R_CSALL_B</td> <td>O</td> </tr> <tr> <td>syscik_sel[4]</td> <td>EXT_SYSCCLK</td> <td>I</td> </tr> <tr> <td>sft_cfg7[11:8]=4'b0010</td> <td>EXT_CLK27</td> <td>I</td> </tr> <tr> <td>fm_qpio_len[3:0]>3</td> <td>FM_GPIOB[6]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_F[0]</td> <td>I</td> </tr> <tr> <td>sft_cfg7[13:12]=2'b11</td> <td>CLK54_OUT</td> <td>O</td> </tr> <tr> <td>sft_cfg9[14:13]=2'b11</td> <td>EXT_CLK48</td> <td>I</td> </tr> <tr> <td>sft_cfg6[4]=1'b1</td> <td>DELAY_CHAIN3</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[15] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[5:4]=2'b10	UA1_TXD	O	sft_cfg[8:6]=3'b001	R_CSALL_B	O	syscik_sel[4]	EXT_SYSCCLK	I	sft_cfg7[11:8]=4'b0010	EXT_CLK27	I	fm_qpio_len[3:0]>3	FM_GPIOB[6]	I/O	sft_cfg8[9]=1'b1	DAC_DATA_F[0]	I	sft_cfg7[13:12]=2'b11	CLK54_OUT	O	sft_cfg9[14:13]=2'b11	EXT_CLK48	I	sft_cfg6[4]=1'b1	DELAY_CHAIN3	O	(other)	GPIO[15] (default)	I/O
			Priority selection	Function	Dir																															
			sft_cfg2[5:4]=2'b10	UA1_TXD	O																															
			sft_cfg[8:6]=3'b001	R_CSALL_B	O																															
			syscik_sel[4]	EXT_SYSCCLK	I																															
			sft_cfg7[11:8]=4'b0010	EXT_CLK27	I																															
			fm_qpio_len[3:0]>3	FM_GPIOB[6]	I/O																															
			sft_cfg8[9]=1'b1	DAC_DATA_F[0]	I																															
			sft_cfg7[13:12]=2'b11	CLK54_OUT	O																															
			sft_cfg9[14:13]=2'b11	EXT_CLK48	I																															
sft_cfg6[4]=1'b1	DELAY_CHAIN3	O																																		
(other)	GPIO[15] (default)	I/O																																		
R_CS4_B/GPIO	66	IO	ROM / SRAM / flash chip select #4 or GPIO																																	
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg1[3]=1'b1</td> <td>R_CS4_B (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg1[7]=1'b1 & fm_qpio_len[3:0]=10,11,12</td> <td>FM_GPIOB[20]</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_E[9]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[16]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg1[3]=1'b1	R_CS4_B (default)	O	sft_cfg1[7]=1'b1 & fm_qpio_len[3:0]=10,11,12	FM_GPIOB[20]	I/O	sft_cfg8[9]=1'b1	DAC_DATA_E[9]	I	(other)	GPIO[16]	I/O																		
			Priority selection	Function	Dir																															
			sft_cfg1[3]=1'b1	R_CS4_B (default)	O																															
			sft_cfg1[7]=1'b1 & fm_qpio_len[3:0]=10,11,12	FM_GPIOB[20]	I/O																															
sft_cfg8[9]=1'b1	DAC_DATA_E[9]	I																																		
(other)	GPIO[16]	I/O																																		
R_CS3_B/GPIO	67	IO	ROM / SRAM / flash chip select #3 or GPIO																																	
			<table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg1[2]=1'b1</td> <td>R_CS3_B (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_E[8]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[17]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg1[2]=1'b1	R_CS3_B (default)	O	sft_cfg8[9]=1'b1	DAC_DATA_E[8]	I	(other)	GPIO[17]	I/O																					
			Priority selection	Function	Dir																															
			sft_cfg1[2]=1'b1	R_CS3_B (default)	O																															
sft_cfg8[9]=1'b1	DAC_DATA_E[8]	I																																		
(other)	GPIO[17]	I/O																																		

Symbol	Pin NO	I/O	Description												
R_CS2_B/GPIO	68	IO	ROM / SRAM / flash chip select #2 or GPIO <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg1[1]=1'b1</td> <td>R_CS2_B (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_E[7]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[18]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg1[1]=1'b1	R_CS2_B (default)	O	sft_cfg8[9]=1'b1	DAC_DATA_E[7]	I	(other)	GPIO[18]	I/O
Priority selection	Function	Dir													
sft_cfg1[1]=1'b1	R_CS2_B (default)	O													
sft_cfg8[9]=1'b1	DAC_DATA_E[7]	I													
(other)	GPIO[18]	I/O													
R_CS1_B/GPIO	69	IO	ROM / SRAM / flash chip select #1 or GPIO <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg1[0]=1'b1</td> <td>R_CS1_B (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_E[6]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[19]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg1[0]=1'b1	R_CS1_B (default)	O	sft_cfg8[9]=1'b1	DAC_DATA_E[6]	I	(other)	GPIO[19]	I/O
Priority selection	Function	Dir													
sft_cfg1[0]=1'b1	R_CS1_B (default)	O													
sft_cfg8[9]=1'b1	DAC_DATA_E[6]	I													
(other)	GPIO[19]	I/O													
RST_B	70	I	System reset (active low reset)												
IR_IN/GPIO	71	I	GPIO <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg8[9]=1'b1</td> <td>IR_IN,GPIO[20]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[20] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg8[9]=1'b1	IR_IN,GPIO[20]	I	(other)	GPIO[20] (default)	I/O			
Priority selection	Function	Dir													
sft_cfg8[9]=1'b1	IR_IN,GPIO[20]	I													
(other)	GPIO[20] (default)	I/O													
VFD_CLK/GPIO	72	IO	GPIO[24] for VFD_CLK												
VFD_STB/GPIO	73	IO	GPIO[22] for VFD_STB <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_E[5]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[22] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg8[9]=1'b1	DAC_DATA_E[5]	I	(other)	GPIO[22] (default)	I/O			
Priority selection	Function	Dir													
sft_cfg8[9]=1'b1	DAC_DATA_E[5]	I													
(other)	GPIO[22] (default)	I/O													
VFD_DATA/GPIO	74	IO	GPIO[23] for VFD_DATA <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_E[4]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[22] (default)</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg8[9]=1'b1	DAC_DATA_E[4]	I	(other)	GPIO[22] (default)	I/O			
Priority selection	Function	Dir													
sft_cfg8[9]=1'b1	DAC_DATA_E[4]	I													
(other)	GPIO[22] (default)	I/O													
R_A20	75	IO	ROM / SDRAM / flash address bus bit [20] (216 pin package)												
R_A19 (E_MX11)	76	IO	ROM / SDRAM / flash address bus bit [19]												
CLKIN	77	I	Clock input / crystal in (XTALI)												
CLKOUT	78	O	Clock input / crystal in (XTALO)												
RESERVED_N	79	A	Reserved												
RESERVED_P	80	A	Reserved												
RESERVED	81	A	Reserved												
RESERVED	82	A	Reserved												
VSS_PLLA	83	S	Ground pin for audio PLL												
VDD_PLLA	84	S	3.3V power supply pin for audio PLL												
VSS_PLLV	85	S	Ground pin for system PLL and audio PLL												
VDD_PLLV	86	S	1.8V power supply pin for system PLL												
M_DD[7]	87	IO	SDRAM data bus [7]												
M_DD[6]	88	IO	SDRAM data bus [6]												
M_DD[5]	89	IO	SDRAM data bus [5]												
M_DD[4]	90	IO	SDRAM data bus [4]												
M_DD[3]	91	IO	SDRAM data bus [3]												
VDD_02	92	S	I/O power supply #2												
M_DD[2]	93	IO	SDRAM data bus [2]												
M_DD[1]	94	IO	SDRAM data bus [1]												
M_DD[0]	95	IO	SDRAM data bus [0]												
M_WE_B	96	IO	SDRAM write enable / row precharge												
M_CAS_B	97	IO	SDRAM column address strobe (CASB)												
M_RAS_B	98	IO	SDRAM column address strobe (RASB)												
VSS_O2/VSS_K2	99	S	Kernel logic / I/O power shared ground supply #2												

Symbol	Pin NO	I/O	Description															
M_CS0_B/GPIO	100	IO	SDRAM chip select 0, or GPIO[24] <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg0[0]=1'b1</td> <td>SDRAM chip select (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_D[2]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[24]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg0[0]=1'b1	SDRAM chip select (default)	O	sft_cfg8[9]=1'b1	DAC_DATA_D[2]	I	(other)	GPIO[24]	I/O			
Priority selection	Function	Dir																
sft_cfg0[0]=1'b1	SDRAM chip select (default)	O																
sft_cfg8[9]=1'b1	DAC_DATA_D[2]	I																
(other)	GPIO[24]	I/O																
M_BAO	101	IO	SDRAM bank select address [0]															
M_DD[15]	102	IO	SDRAM data bus [15]															
M_DD[14]	103	IO	SDRAM data bus [14]															
M_DD[13]	104	IO	SDRAM data bus [13]															
VDD_K2	105	S	Kernel logic power supply#2															
M_DD[12]	106	IO	SDRAM data bus [12]															
M_DD[11]	107	IO	SDRAM data bus [11]															
M_DD[10]	108	IO	SDRAM data bus [10]															
M_DD[9]	109	IO	SDRAM data bus [9]															
M_DD[8]	110	IO	SDRAM data bus [8]															
M_A[11]/GPIO	111	IO	SDRAM address bus [11] or GPIO [25] <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg1[4]=1'b1</td> <td>SDRAM address bus M_A[11] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_C[2]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[25]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg1[4]=1'b1	SDRAM address bus M_A[11] (default)	O	sft_cfg8[9]=1'b1	DAC_DATA_C[2]	I	(other)	GPIO[25]	I/O			
Priority selection	Function	Dir																
sft_cfg1[4]=1'b1	SDRAM address bus M_A[11] (default)	O																
sft_cfg8[9]=1'b1	DAC_DATA_C[2]	I																
(other)	GPIO[25]	I/O																
VDD_03	112	S	I/O power supply #3															
M_CLKO	113	O	SDRAM clock output															
VSS_03/VSS_K3	114	S	Kernel logic/I/O power shared ground supply #3															
M_CKE/GPIO	115	IO	SDRAM clock enable, or gpio[26] <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg0[1]=1'b1</td> <td>DRAM clock enable (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_C[1]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[26]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg0[1]=1'b1	DRAM clock enable (default)	O	sft_cfg8[9]=1'b1	DAC_DATA_C[1]	I	(other)	GPIO[26]	I/O			
Priority selection	Function	Dir																
sft_cfg0[1]=1'b1	DRAM clock enable (default)	O																
sft_cfg8[9]=1'b1	DAC_DATA_C[1]	I																
(other)	GPIO[26]	I/O																
M_A[9]	116	IO	SDRAM address bus [9]															
M_A[8]	117	IO	SDRAM address bus [8]															
M_A[7]	118	IO	SDRAM address bus [7]															
M_A[6]	119	I/O	SDRAM address bus [6]															
M_A[5]	120	I/O	SDRAM address bus [5]															
VDD_K3	121	S	Kernel logic power supply #3															
M_A[4]	122	I/O	SDRAM address bus [4]															
M_DQM1/GPIO	123	I/O	SDRAM data input/output mask for M_DD[15:8] or GPIOA[27]															
M_DQM0/GPIO	124	I/O	SDRAM data input/output mask for M_DD[7:0] or GPIOA[28] <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg0[2]</td> <td>SDRAM data input/output mask for M_DD[7,8] (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_D_R[5]</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_B[3]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[28]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg0[2]	SDRAM data input/output mask for M_DD[7,8] (default)	I/O	sft_cfg8[8]=1'b1	ADC_MONO_D_R[5]	O	sft_cfg8[9]=1'b1	DAC_DATA_B[3]	I	(other)	GPIO[28]	I/O
Priority selection	Function	Dir																
sft_cfg0[2]	SDRAM data input/output mask for M_DD[7,8] (default)	I/O																
sft_cfg8[8]=1'b1	ADC_MONO_D_R[5]	O																
sft_cfg8[9]=1'b1	DAC_DATA_B[3]	I																
(other)	GPIO[28]	I/O																
M_BA1/GPIO	125	I/O	SDRAM bank select address [1] or GPIOA[29] <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg0[6]=1'b1</td> <td>SDRAM bank select address [1] (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_D_R[6]</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_DATA_B[2]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[29]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg0[6]=1'b1	SDRAM bank select address [1] (default)	I/O	sft_cfg8[8]=1'b1	ADC_MONO_D_R[6]	O	sft_cfg8[9]=1'b1	DAC_DATA_B[2]	I	(other)	GPIO[29]	I/O
Priority selection	Function	Dir																
sft_cfg0[6]=1'b1	SDRAM bank select address [1] (default)	I/O																
sft_cfg8[8]=1'b1	ADC_MONO_D_R[6]	O																
sft_cfg8[9]=1'b1	DAC_DATA_B[2]	I																
(other)	GPIO[29]	I/O																

Symbol	Pin NO	I/O	Description																																									
M_A[10]	126	O	SDRAM address bus [10]																																									
M_A[0]	127	O	SDRAM address bus [0]																																									
VSS_04/VSS_K4	128	S	Kernel logic / I/O power started around supply #4																																									
M_A[1]	129	O	SDRAM address bus [1]																																									
M_A[2]	130	O	SDRAM address bus [2]																																									
M_A[3]	131	O	SDRAM address bus [3]																																									
R_WE_B	132	I/O	ROM / SRAM / flash write strobe																																									
R_A17	133	I/O	ROM / SRAM / flash address bus bit [17]																																									
R_A14	134	I/O	ROM / SRAM / flash address bus bit [14]																																									
R_A13	135	I/O	ROM / SRAM / flash address bus bit [13]																																									
VDD_04	136	S	I/O power supply #4																																									
R_A8	137	O	ROM / SRAM / flash address bus bit [8]																																									
R_A9	138	O	ROM / SRAM / flash address bus bit [9]																																									
R_A11	139	I/O	ROM / SRAM / flash address bus bit [11]																																									
R_A10	140	O	ROM / SRAM / flash address bus bit [10]																																									
M_DQM3/GPIO	141	I/O	SDRAM data input/output mask for M_DD[31:24] or GPIOA[38] <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg0[5]=1'b1</td> <td>SDRAM data input/output mask for M_DD[31:24] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg2[3:2]=2'b11</td> <td>UAC_RXD</td> <td>I</td> </tr> <tr> <td>sft_cfg1[8:6]=3'b011</td> <td>R_CSALL_B</td> <td>O</td> </tr> <tr> <td>sft_cfg3[13:12]=2'b10</td> <td>TV_HSYNC</td> <td>I/O</td> </tr> <tr> <td>sft_cfg4[15:13]=3'b010</td> <td>TV_HSYNC_PC</td> <td>O</td> </tr> <tr> <td>sft_cfg7[7:6]=2'b01</td> <td>PCMCIA_IOW_B</td> <td>O</td> </tr> <tr> <td>sft_cfg0[13:12]=2'b01</td> <td>TV_LCD_G[2]</td> <td>O</td> </tr> <tr> <td>sft_cfg7[1]=1'b0</td> <td rowspan="3">FM_GPIOB[19]</td> <td rowspan="3">I/O</td> </tr> <tr> <td>sft_cfg0[11]=1'b0</td> </tr> <tr> <td>fm_gpio_lan[13:0]>9</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_D_L[5]</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_OPA[1]</td> <td>I</td> </tr> <tr> <td>sft_cfg8[10]=1'b1</td> <td>OGT_BIST_FAIL</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[38]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg0[5]=1'b1	SDRAM data input/output mask for M_DD[31:24] (default)	O	sft_cfg2[3:2]=2'b11	UAC_RXD	I	sft_cfg1[8:6]=3'b011	R_CSALL_B	O	sft_cfg3[13:12]=2'b10	TV_HSYNC	I/O	sft_cfg4[15:13]=3'b010	TV_HSYNC_PC	O	sft_cfg7[7:6]=2'b01	PCMCIA_IOW_B	O	sft_cfg0[13:12]=2'b01	TV_LCD_G[2]	O	sft_cfg7[1]=1'b0	FM_GPIOB[19]	I/O	sft_cfg0[11]=1'b0	fm_gpio_lan[13:0]>9	sft_cfg8[8]=1'b1	ADC_MONO_D_L[5]	O	sft_cfg8[9]=1'b1	DAC_OPA[1]	I	sft_cfg8[10]=1'b1	OGT_BIST_FAIL	O	(other)	GPIO[38]	I/O
Priority selection	Function	Dir																																										
sft_cfg0[5]=1'b1	SDRAM data input/output mask for M_DD[31:24] (default)	O																																										
sft_cfg2[3:2]=2'b11	UAC_RXD	I																																										
sft_cfg1[8:6]=3'b011	R_CSALL_B	O																																										
sft_cfg3[13:12]=2'b10	TV_HSYNC	I/O																																										
sft_cfg4[15:13]=3'b010	TV_HSYNC_PC	O																																										
sft_cfg7[7:6]=2'b01	PCMCIA_IOW_B	O																																										
sft_cfg0[13:12]=2'b01	TV_LCD_G[2]	O																																										
sft_cfg7[1]=1'b0	FM_GPIOB[19]	I/O																																										
sft_cfg0[11]=1'b0																																												
fm_gpio_lan[13:0]>9																																												
sft_cfg8[8]=1'b1	ADC_MONO_D_L[5]	O																																										
sft_cfg8[9]=1'b1	DAC_OPA[1]	I																																										
sft_cfg8[10]=1'b1	OGT_BIST_FAIL	O																																										
(other)	GPIO[38]	I/O																																										
M_DQM2/GPIO	142	I/O	SDRAM data input/output mask for M_DD[31:24] or GPIO[39] <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg0[4]=1'b1</td> <td>SDRAM data input/output mask for M_DD[23:16] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg2[8:2]=2'b11</td> <td>UA0_TXD</td> <td>O</td> </tr> <tr> <td>sft_cfg3[13:12]=2'b10</td> <td>TV_VSYNC</td> <td>I/O</td> </tr> <tr> <td>sft_cfg4[15:13]=3'b010</td> <td>TV_VSYNC_PC</td> <td>O</td> </tr> <tr> <td>sft_cfg7[7:6]=2'b01</td> <td>PCMCIA_IOR_B</td> <td>O</td> </tr> <tr> <td>sft_cfg0[13:12]=2'b01</td> <td>TV_LCD_G[3]</td> <td>O</td> </tr> <tr> <td>sft_cfg7[1]=1'b0,</td> <td rowspan="3">FM_GPIOB[18]</td> <td rowspan="3">I/O</td> </tr> <tr> <td>sft_cfg0[11]=1'b0,</td> </tr> <tr> <td>fm_gpio_len[3:0]>9</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_D_L[6]</td> <td>O</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_OPA[2]</td> <td>I</td> </tr> <tr> <td>sft_cfg8[10]=1'b1</td> <td>BUF_CTRL_BIST_FAIL</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[39]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg0[4]=1'b1	SDRAM data input/output mask for M_DD[23:16] (default)	O	sft_cfg2[8:2]=2'b11	UA0_TXD	O	sft_cfg3[13:12]=2'b10	TV_VSYNC	I/O	sft_cfg4[15:13]=3'b010	TV_VSYNC_PC	O	sft_cfg7[7:6]=2'b01	PCMCIA_IOR_B	O	sft_cfg0[13:12]=2'b01	TV_LCD_G[3]	O	sft_cfg7[1]=1'b0,	FM_GPIOB[18]	I/O	sft_cfg0[11]=1'b0,	fm_gpio_len[3:0]>9	sft_cfg8[8]=1'b1	ADC_MONO_D_L[6]	O	sft_cfg8[9]=1'b1	DAC_OPA[2]	I	sft_cfg8[10]=1'b1	BUF_CTRL_BIST_FAIL	O	(other)	GPIO[39]	I/O			
Priority selection	Function	Dir																																										
sft_cfg0[4]=1'b1	SDRAM data input/output mask for M_DD[23:16] (default)	O																																										
sft_cfg2[8:2]=2'b11	UA0_TXD	O																																										
sft_cfg3[13:12]=2'b10	TV_VSYNC	I/O																																										
sft_cfg4[15:13]=3'b010	TV_VSYNC_PC	O																																										
sft_cfg7[7:6]=2'b01	PCMCIA_IOR_B	O																																										
sft_cfg0[13:12]=2'b01	TV_LCD_G[3]	O																																										
sft_cfg7[1]=1'b0,	FM_GPIOB[18]	I/O																																										
sft_cfg0[11]=1'b0,																																												
fm_gpio_len[3:0]>9																																												
sft_cfg8[8]=1'b1	ADC_MONO_D_L[6]	O																																										
sft_cfg8[9]=1'b1	DAC_OPA[2]	I																																										
sft_cfg8[10]=1'b1	BUF_CTRL_BIST_FAIL	O																																										
(other)	GPIO[39]	I/O																																										
VDD_K4	143	S	Kernel logic power supply #4																																									
R_OE_B	144	I/O	ROM / SRAM / flash output enable																																									
R_D7	145	I/O	ROM / SRAM / flash data bus bit [7]																																									
R_D6	146	I/O	ROM / SRAM / flash data bus bit [6]																																									

Symbol	Pin NO	I/O	Description															
R_D5	147	I/O	ROM / SRAM / flash data bus bit [5]															
R_D4	148	I/O	ROM / SRAM / flash data bus bit [4]															
R_D3	149	I/O	ROM / SRAM / flash data bus bit [3]															
VSS_O5/VSS_K5	150	S	Kernel logic / I/O power shared ground supply #5															
R_D2	151	I/O	ROM / SRAM / flash data bus bit [2]															
R_D1	152	I/O	ROM / SRAM / flash data bus bit [1]															
R_D0	153	I/O	ROM / SRAM / flash data bus bit [0]															
R_A0	154	O	ROM / SRAM / flash address bus bit [0]															
R_A1	155	O	ROM / SRAM / flash address bus bit [1]															
R_A2	156	O	ROM / SRAM / flash address bus bit [2]															
R_A3	157	O	ROM / SRAM / flash address bus bit [3]															
R_A4	158	O	ROM / SRAM / flash address bus bit [4]															
R_A5	159	O	ROM / SRAM / flash address bus bit [5]															
R_A6	160	O	ROM / SRAM / flash address bus bit [6]															
R_A7	161	O	ROM / SRAM / flash address bus bit [7]															
R_A12	162	I/O	ROM / SRAM / flash address bus bit [12]															
R_A15	163	I/O	ROM / SRAM / flash address bus bit [15]															
AIN/AIN_L	164	A	ADC input (left channel)															
AIN_R	165	A	ADC input (right channel)															
VM	166	A	ADC input voltage reference when not used, connect a 0.1uF to ground.															
VDD_ADA	167	S	3.3V power supply for on-chip audio ADC															
VSS_ADA	168	S	Ground pin for on-chip audio ADC															
R_A16	169	I/O	ROM / SRAM / flash address bus bit [16]															
R_A18	170	I/O	ROM / SRAM / flash address bus bit [18]															
A_IEC_TX/GPIO	171	I/O	IEC 958 transmit data <table border="1" data-bbox="699 1048 1401 1220"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[8]=1'b1</td> <td>A_IEC_TX (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_C[0]</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_OPF[0]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[52]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[8]=1'b1	A_IEC_TX (default)	O	sft_cfg8[8]=1'b1	ADC_MONO_C[0]	I	sft_cfg8[9]=1'b1	DAC_OPF[0]	I	(other)	GPIO[52]	I/O
Priority selection	Function	Dir																
sft_cfg3[8]=1'b1	A_IEC_TX (default)	O																
sft_cfg8[8]=1'b1	ADC_MONO_C[0]	I																
sft_cfg8[9]=1'b1	DAC_OPF[0]	I																
(other)	GPIO[52]	I/O																
A_DATA[0]/GPIO	172	I/O	Serial audio data output for channel 1/0 or GPIO <table border="1" data-bbox="699 1288 1401 1460"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[1]=1'b1</td> <td>A_DATA[0] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_C[1]</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_OPF[1]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[53]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[1]=1'b1	A_DATA[0] (default)	O	sft_cfg8[8]=1'b1	ADC_MONO_C[1]	I	sft_cfg8[9]=1'b1	DAC_OPF[1]	I	(other)	GPIO[53]	I/O
Priority selection	Function	Dir																
sft_cfg3[1]=1'b1	A_DATA[0] (default)	O																
sft_cfg8[8]=1'b1	ADC_MONO_C[1]	I																
sft_cfg8[9]=1'b1	DAC_OPF[1]	I																
(other)	GPIO[53]	I/O																
VDD_O5	173	S	I/O power supply #5															
A_DATA[1]/GPIO	174	I/O	Serial audio data output for channel 3/2 or GPIO <table border="1" data-bbox="699 1563 1401 1736"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[2]=1'b1</td> <td>A_DATA[1] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_C[2]</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_OPF[2]</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[54]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[2]=1'b1	A_DATA[1] (default)	O	sft_cfg8[8]=1'b1	ADC_MONO_C[2]	I	sft_cfg8[9]=1'b1	DAC_OPF[2]	I	(other)	GPIO[54]	I/O
Priority selection	Function	Dir																
sft_cfg3[2]=1'b1	A_DATA[1] (default)	O																
sft_cfg8[8]=1'b1	ADC_MONO_C[2]	I																
sft_cfg8[9]=1'b1	DAC_OPF[2]	I																
(other)	GPIO[54]	I/O																
A_DATA[2]/GPIO	175	I/O	Serial audio data output for channel 5/4 or GPIO <table border="1" data-bbox="699 1803 1401 1975"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[3]=1'b1</td> <td>A_DATA[2] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_PWAD</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_PDALL</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[55]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[3]=1'b1	A_DATA[2] (default)	O	sft_cfg8[8]=1'b1	ADC_MONO_PWAD	I	sft_cfg8[9]=1'b1	DAC_PDALL	I	(other)	GPIO[55]	I/O
Priority selection	Function	Dir																
sft_cfg3[3]=1'b1	A_DATA[2] (default)	O																
sft_cfg8[8]=1'b1	ADC_MONO_PWAD	I																
sft_cfg8[9]=1'b1	DAC_PDALL	I																
(other)	GPIO[55]	I/O																

Symbol	Pin NO	I/O	Description															
A_DATA[3]/GPIO	176	I/O	Serial audio data output for channel 7/6 or GPIO <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[4]=1'b1</td> <td>A_DATA[3] (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_SPGA</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_TEST</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[56]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[4]=1'b1	A_DATA[3] (default)	O	sft_cfg8[8]=1'b1	ADC_MONO_SPGA	I	sft_cfg8[9]=1'b1	DAC_TEST	I	(other)	GPIO[56]	I/O
Priority selection	Function	Dir																
sft_cfg3[4]=1'b1	A_DATA[3] (default)	O																
sft_cfg8[8]=1'b1	ADC_MONO_SPGA	I																
sft_cfg8[9]=1'b1	DAC_TEST	I																
(other)	GPIO[56]	I/O																
A_LRCK/GPIO	177	I/O	PCM data output L/R strobe <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[6]=1'b1</td> <td>A_LRCK (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_MODE1</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_UD</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[57]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[6]=1'b1	A_LRCK (default)	I/O	sft_cfg8[8]=1'b1	ADC_MONO_MODE1	I	sft_cfg8[9]=1'b1	DAC_UD	I	(other)	GPIO[57]	I/O
Priority selection	Function	Dir																
sft_cfg3[6]=1'b1	A_LRCK (default)	I/O																
sft_cfg8[8]=1'b1	ADC_MONO_MODE1	I																
sft_cfg8[9]=1'b1	DAC_UD	I																
(other)	GPIO[57]	I/O																
VSS_O6/VSS_K6	178	S	Kernel logic I/O power shard ground supply #6															
A_BCK/GPIO	179	I/O	PCM bit clock <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[0]=1'b1</td> <td>A_BCK (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_MODE1_1</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_BGPD</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[58]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[0]=1'b1	A_BCK (default)	I/O	sft_cfg8[8]=1'b1	ADC_MONO_MODE1_1	I	sft_cfg8[9]=1'b1	DAC_BGPD	I	(other)	GPIO[58]	I/O
Priority selection	Function	Dir																
sft_cfg3[0]=1'b1	A_BCK (default)	I/O																
sft_cfg8[8]=1'b1	ADC_MONO_MODE1_1	I																
sft_cfg8[9]=1'b1	DAC_BGPD	I																
(other)	GPIO[58]	I/O																
A_BCK/GPIO	180	I/O	Audio over-sampling clock <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg3[9]=1'b1</td> <td>A_XCK (default)</td> <td>I/O</td> </tr> <tr> <td>sft_cfg8[8]=1'b1</td> <td>ADC_MONO_MODE2</td> <td>I</td> </tr> <tr> <td>sft_cfg8[9]=1'b1</td> <td>DAC_CLK</td> <td>I</td> </tr> <tr> <td>(other)</td> <td>GPIO[59]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg3[9]=1'b1	A_XCK (default)	I/O	sft_cfg8[8]=1'b1	ADC_MONO_MODE2	I	sft_cfg8[9]=1'b1	DAC_CLK	I	(other)	GPIO[59]	I/O
Priority selection	Function	Dir																
sft_cfg3[9]=1'b1	A_XCK (default)	I/O																
sft_cfg8[8]=1'b1	ADC_MONO_MODE2	I																
sft_cfg8[9]=1'b1	DAC_CLK	I																
(other)	GPIO[59]	I/O																
UA0_RX/GPIO	181	I/O	UART #0 data receive or GPIO <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[3:2]=2'b01</td> <td>UART0_RX (default)</td> <td>I</td> </tr> <tr> <td>sft_cfg3[13:12]=2'b01</td> <td>TV_HSYNC</td> <td>I/O</td> </tr> <tr> <td>sft_cfg4[15:13]=3'b011</td> <td>HSYNC_PC</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[60]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[3:2]=2'b01	UART0_RX (default)	I	sft_cfg3[13:12]=2'b01	TV_HSYNC	I/O	sft_cfg4[15:13]=3'b011	HSYNC_PC	O	(other)	GPIO[60]	I/O
Priority selection	Function	Dir																
sft_cfg2[3:2]=2'b01	UART0_RX (default)	I																
sft_cfg3[13:12]=2'b01	TV_HSYNC	I/O																
sft_cfg4[15:13]=3'b011	HSYNC_PC	O																
(other)	GPIO[60]	I/O																
UA0_TX/GPIO	182	I/O	UART #0 data transmit or GPIO <table border="1"> <thead> <tr> <th>Priority selection</th> <th>Function</th> <th>Dir</th> </tr> </thead> <tbody> <tr> <td>sft_cfg2[3:2]=2'b01</td> <td>UART0_TX (default)</td> <td>O</td> </tr> <tr> <td>sft_cfg3[13:12]=2'b01</td> <td>TV_VSYNC</td> <td>I/O</td> </tr> <tr> <td>sft_cfg4[15:13]=3'b011</td> <td>VSYNC_PC</td> <td>O</td> </tr> <tr> <td>(other)</td> <td>GPIO[61]</td> <td>I/O</td> </tr> </tbody> </table>	Priority selection	Function	Dir	sft_cfg2[3:2]=2'b01	UART0_TX (default)	O	sft_cfg3[13:12]=2'b01	TV_VSYNC	I/O	sft_cfg4[15:13]=3'b011	VSYNC_PC	O	(other)	GPIO[61]	I/O
Priority selection	Function	Dir																
sft_cfg2[3:2]=2'b01	UART0_TX (default)	O																
sft_cfg3[13:12]=2'b01	TV_VSYNC	I/O																
sft_cfg4[15:13]=3'b011	VSYNC_PC	O																
(other)	GPIO[61]	I/O																
V_COMP	183	A	Compensation pin. A 0.1pF ceramic capacitor must be used to bypass this pin to VSSA. The lead length must be kept as short as possible to avoid noise.															
V_BIAS	184																	
V_FSADJ	185	A	Full-Scale adjustment control pin. The full-scale current of D/A converters can be adjusted by connecting a resistor (Rset) between this pin and ground.															
V_REFOUT	186	A	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive V_REFIN pin directly.															

Symbol	Pin NO	I/O	Description
V_DAC[0]	187	A	Video DAC output #0. This is a high-impedance current source output. These outputs can drive a 37.5Ω load directly.
VDD_TVA0	188	S	TV_DAC power supply #0
VSS_TVA0	189	S	TV_DAC ground pin #0
VDD_TVA1	190	S	TV_DAC power supply #1
VSS_TVA1	191	S	TV_DAC ground pin #1
V_DAC[3]	192	A	Video DAC output #3. This is a high-impedance current source output. These outputs can drive a 37.5Ω load directly.
V_DAC[4]	193	A	Video DAC output #4. This is a high-impedance current source output. These outputs can drive a 37.5Ω load directly.
VDD_TVA2	194	S	TV_DAC power supply #2
V_DAC[5]	195	A	Video DAC output #5. This is a high-impedance current source output. These outputs can drive a 37.5Ω load directly.
VSS_TVA2	196	S	TV_DAC ground pin #2
PLL_AVDD	197	S	Servo PLL 3.3V power.
LPFO	198	A	NC pin
LPFN	199	A	NC pin
VREFO	200	A	
PDFLT	201	A	
FDFLT	202	A	
LPFNIN	203	A	
LGIN	204	A	
PLL_DS_AVSS	205	S	Servo PLL/Data-slicer ground.
RFI	206	A	
CNIN	207	A	
SLVL	208	A	
DS_AVDD	209	S	Servo Data slicer 3.3V power.
RF_AVDD	210	S	Servo RF 3.3V power.
GMRES	211	A	External reference resistor input.
AGCCAP	212	A	External AGC capacitor connected to ground.
RFRP	213	O	RFRP signal output.
RFO	214	O	RF signal output.
FLTIP	215	I	Differential RF equalizer input #P.
FLTIN	216	I	Differential RF equalizer input #N.

DV-SL800W

IC104, EEPROM 2K BIT 2-WIRE SERIAL

DESCRIPTION:

The Turbo IC 24C01/24C02 is a serial 1K/2K EEPROM fabricated with Turbo's proprietary, high reliability, high performance CMOS technology. It's 1K/2K of memory is configured as 16/32 pages with each page containing 8 bytes. This device offers significant advantages in low power applications.

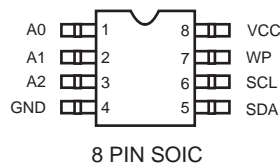
The Turbo IC 24C01/24C02 uses the PC addressing protocol and 2-wire serial interface which includes a bidirectional serial data bus synchronized by a clock. It offers a flexible byte write and a faster 8-byte page write.

The Turbo IC 24C01/24C02 is assembled in either a 8-pin PDIP or 8-pin SOIC package. Pin #1 is the A0 device address input for the device. Pin#2 is the A1 device address input for the device. Pin #3 is the A2 device address input for the device, such that a total of eight 24C01/24C02 devices can be connected on a single bus. Pin #4 is the ground (Vss). Pin #5 is the serial data (SDA) pin used for

bidirectional transfer of data. Pin#6 is the serial clock (SCL) input pin. Pin #7 is the write protect (WP) pin used to be protect hardware data. Pin#8 is the power supply (Vcc) pin.

All data is serially transmitted in bytes (8 bits) on the SDA bus. To access the Turbo IC24C01/24C02 (slave) for a read or write operation, the controller (master) issues a start condition by pulling SDA from high to low while SCL is high. The master then issues the device address byte which consists of 1010(A2)(A1)(A0)(RW). The most significant bits(1010) are a device type code signifying an EEPROM device. A0,A1,and A2 are the device address select bits which has to match the A0,A1,and A2 pin inputs on the device. The B[7] bit (or B[6] bit in the 24C01) is the most significant bit of the memory address. The read/write bit determines whether to do a read or write operation. After each byte is transmitted , the receiver has to provide an acknowledge by pulling the SDA bus low on the ninth clock cycle. The acknowledge is a handshake signal to the transmitter indicating a successful data transmission.

Pin Description:



PIN DESCRIPTION:

DEVICE ADDRESS (A0 & A1 & A2).

A0, A1, and A2 are device address inputs that enables a total of eight 24C02 devices to connect on a simple bus, if the address input pin is left unconnected, it is interpreted as zero.

WRITE PROTECT(WP)

When the write protect input is connected to Vcc, the entire memory array is protected against write operations. For normal write operations, the write protect pin should be grounded, When the pin is left unconnected. WP is interpreted as zero.

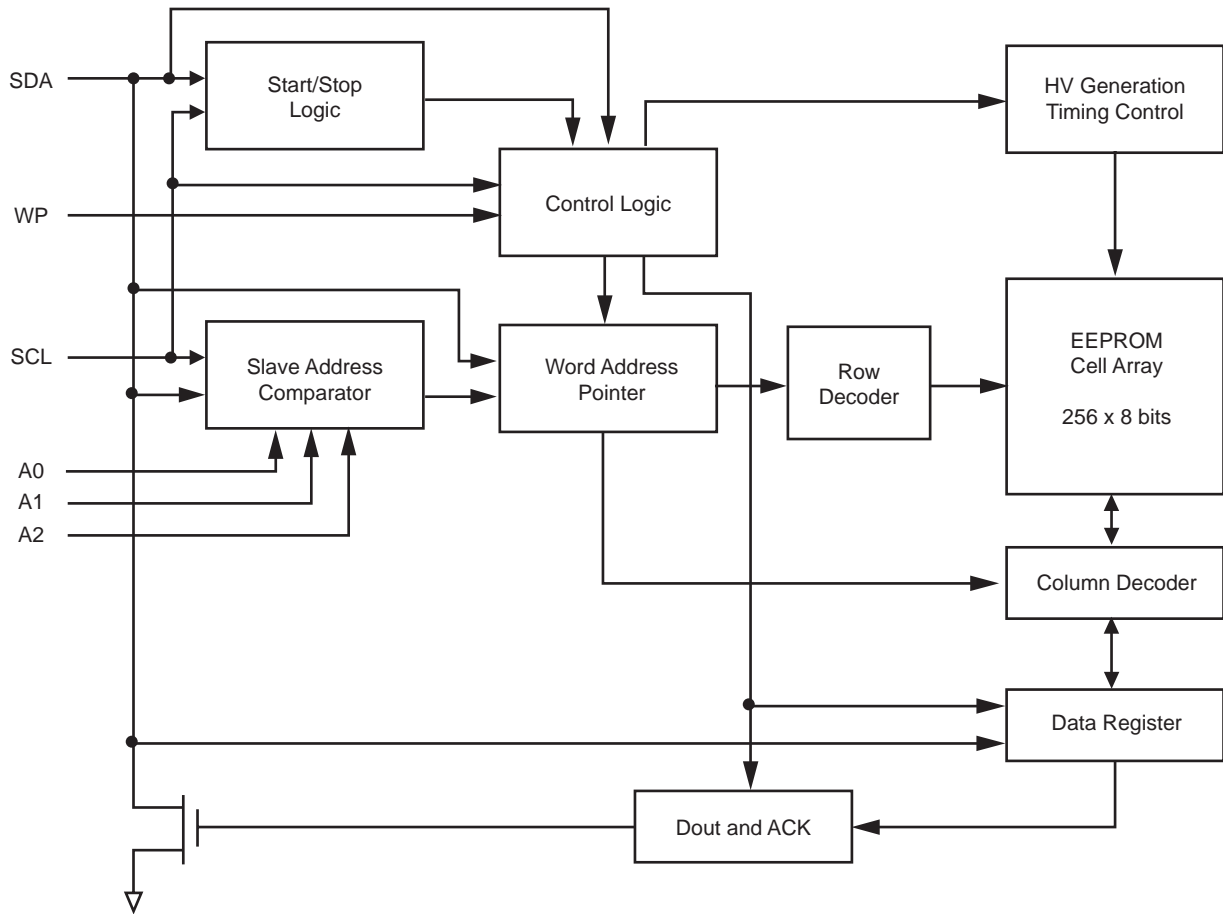
SERIAL DATA(SDA)

SDA is a bidirectional pin used to transfer data in and out of the Turbo IC24C01/24C02. The pin is an open-drain output. A pullup resistor must be connected from SDA to Vcc.

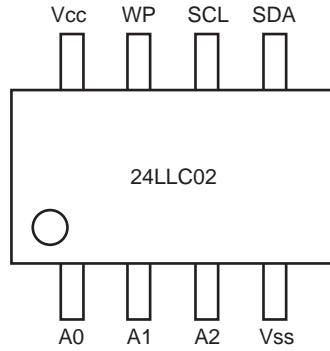
SERIAL CLOCK(SCL)

The SCL input synchronizes the data on the SDA bus. It is used in conjunction with SDA to define the start and stop conditions. It is also used in conjunction with SDA to transfer data to and from the Turbo IC 24C01/24C02.

IC104, 2K BIT SERIAL EEPROM (24LL02A)



IC104, 2K BIT SERIAL EEPROM (24LL02A)



Note: The 24LLC02 is available in 8-pin DIP, SOP, TSSOP package

Figure 1: PIN ASSIGNMENT DIAGRAM

Table Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the Vcc or Vss of the device. These pins are internally pulled down to Vss.	1
Vss	-	Ground pin	-
SDA	I/O	Bi-directional data pin for the I ² C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to Vcc. Typical values for this pull-up resistor are 4.7 kΩ (100 kHz) and 1 kΩ (400 kHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to Vcc, the write function is disabled to protect previously written data in the entire memory; if you tie it to Vss, the write function is enabled. This pin is internally pulled down to Vss.	1
Vcc	-	Single power supply.	-

IC104, 2K BIT SERIAL EEPROM (24LL02A)

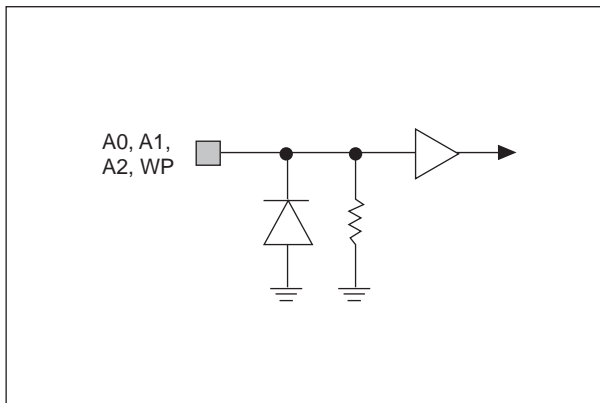


Figure 2: PIN CIRCUIT TYPE 1

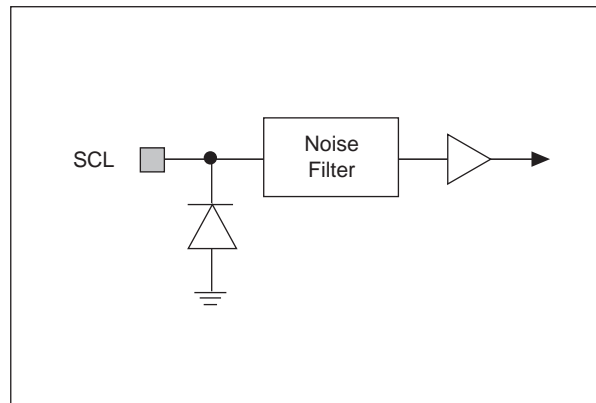


Figure 3: PIN CIRCUIT TYPE 2

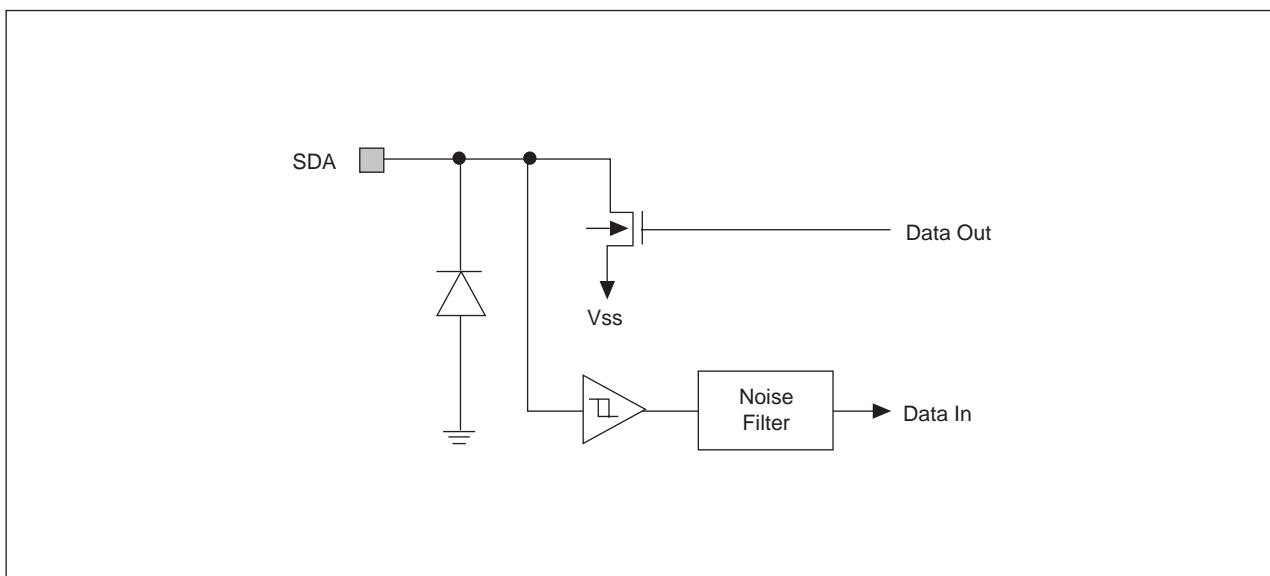
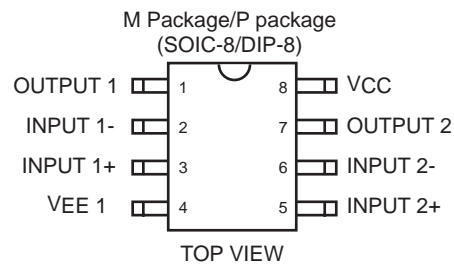


Figure 4: PIN CIRCUIT TYPE 3

DV-SL800W

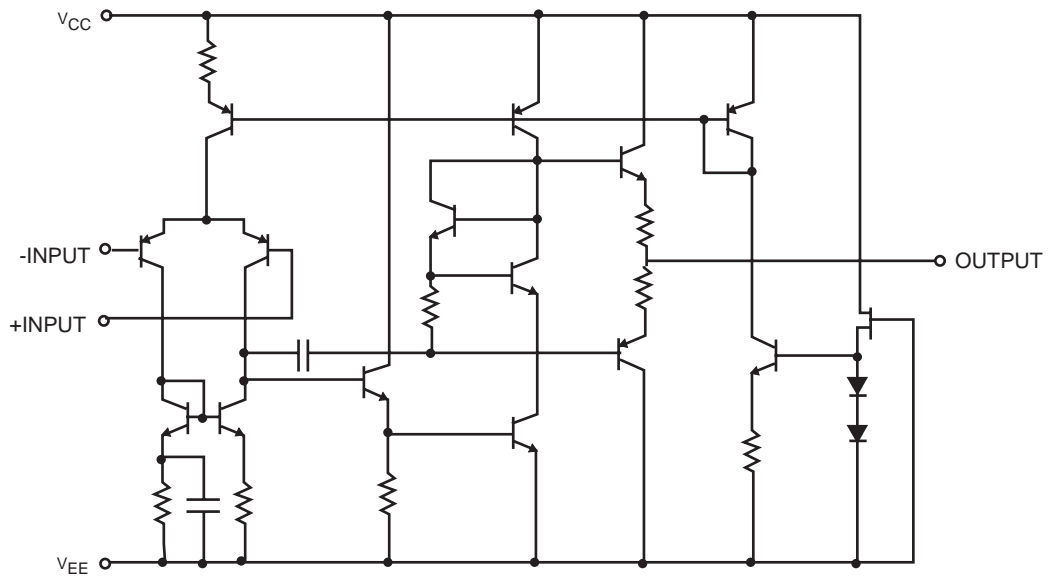
IC1 & IC402, DUAL LOW NOISE OPERATIONAL AMP

Pin Configuration:



Pin Configuration of AZ4558A

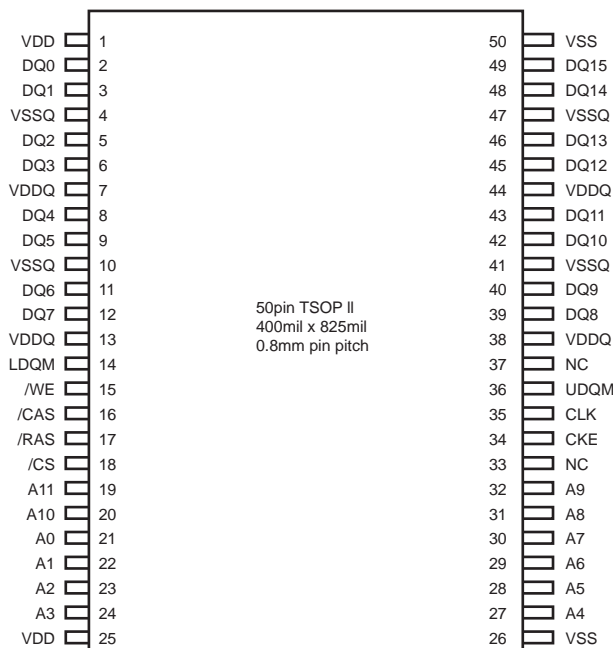
Functional Block Diagram:



Representative Schematic Diagram of AZ4558A (Each Amplifier)

IC106 & IC107, COMS DRAM 143MHZ 16MB

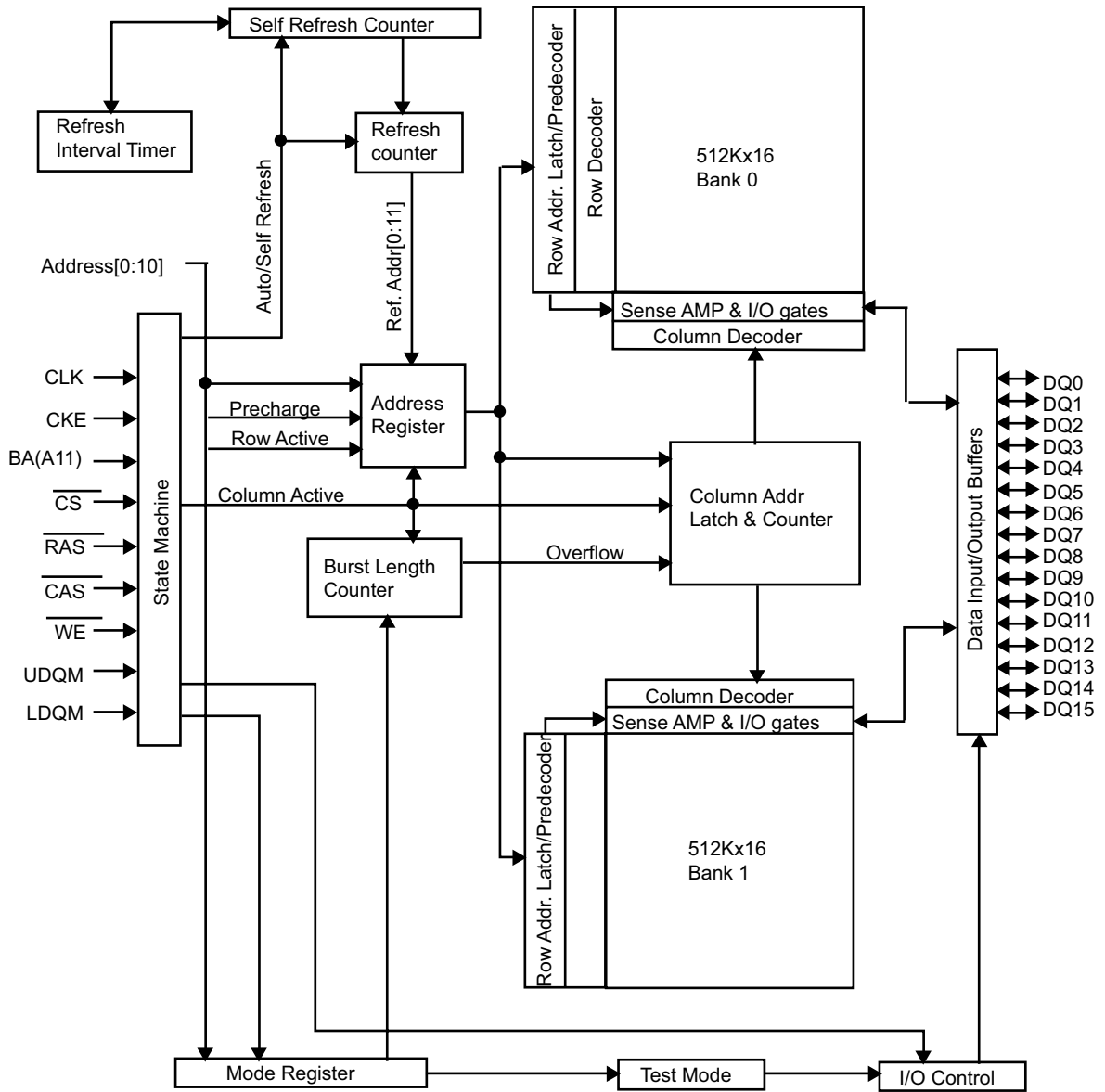
Pin Configuration:



Pin Description:

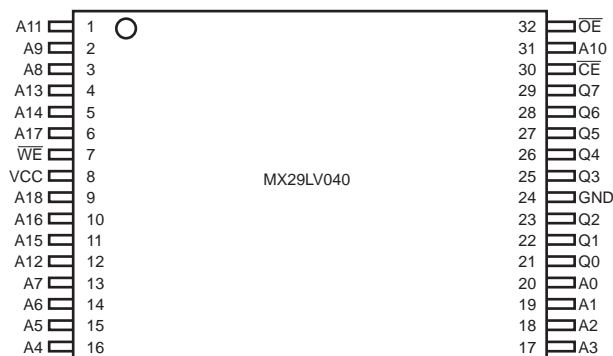
Pin	Pin Name	Description
CLK	Clock	The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
$\overline{\text{CS}}$	Chip Select	Command input enable or mask except CLK, CKE and DQM.
BA	Bank Address	Select either one of banks during both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ activity.
A0 ~ A10	Address	Row Address: RAD ~ RA10, Column Address: CA0 ~ CA7 Auto-precharge flag: A10
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation. Refer function truth table for details.
LDQM, UDQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode.
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input/output pin.
VDD/VSS	Power Supply/Ground	Power supply for internal circuit and input buffer
VDDQ/VSSQ	Data Output Power/Ground	Power supply for DQ
NC	No Connection	No connection

Functional Block Diagram:



IC103A, CMOS 3V 4M FLASH MEMORY

Pin Configurations:

**SECTOR STRUCTURE**

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

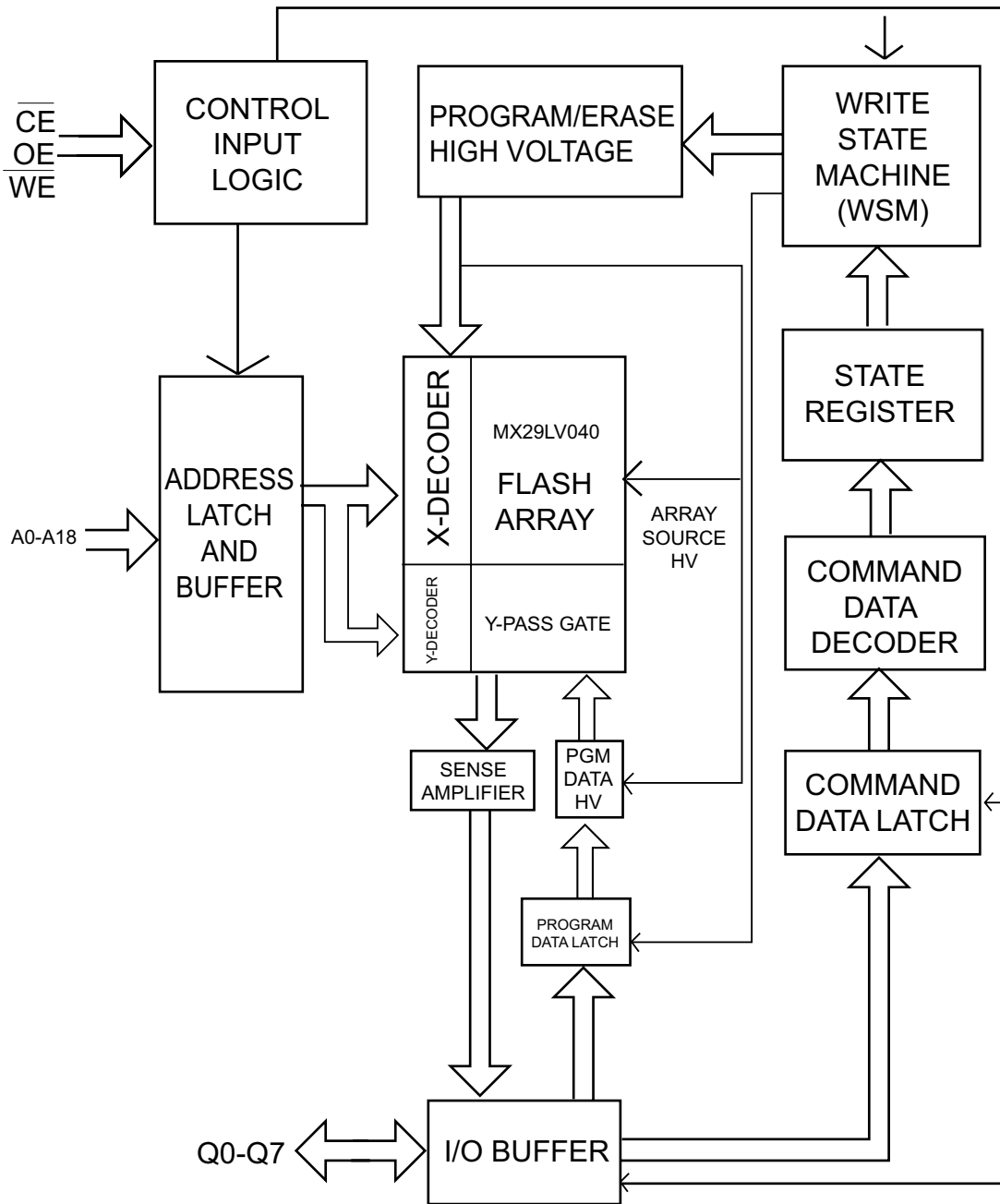
Note: All sectors are 64 Kbytes in size.

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
GND	Ground Pin
VCC	+3.0V single power supply

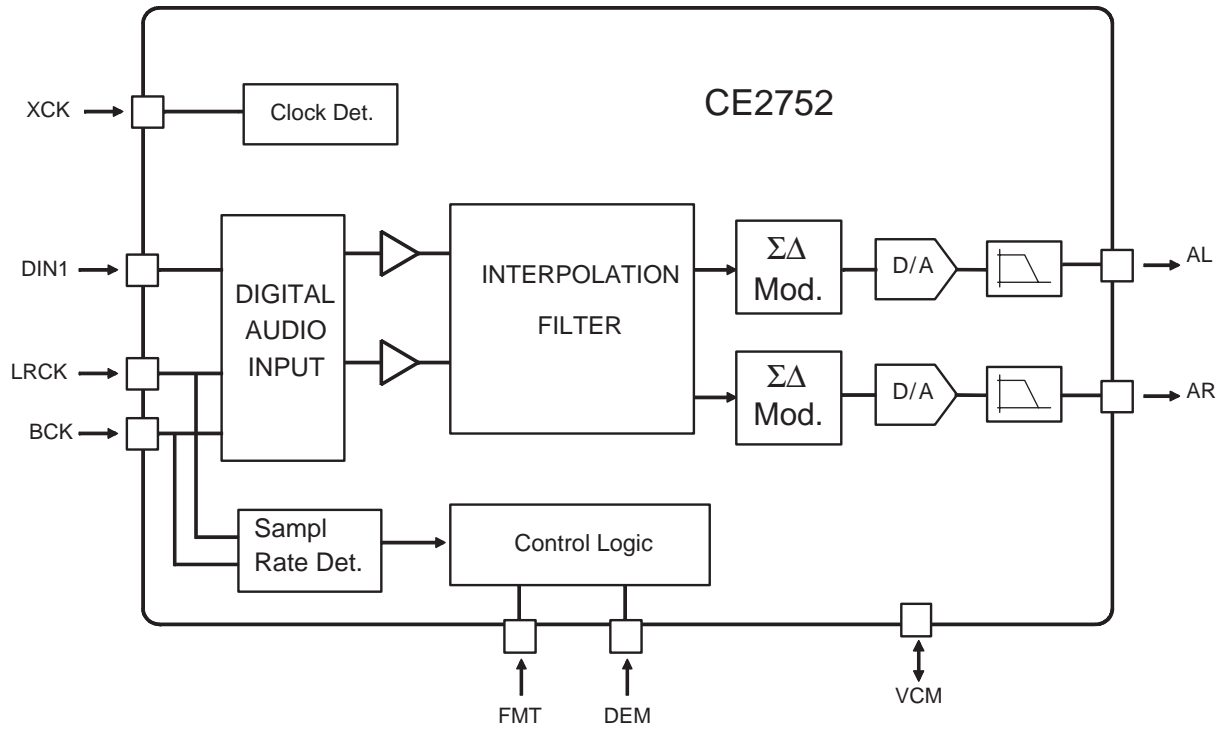
IC103A, CMOS 3V 4M FLASH MEMORY

Block Diagram:



IC401B, STEREO AUDIO DAC, 24-bit, 192kHz

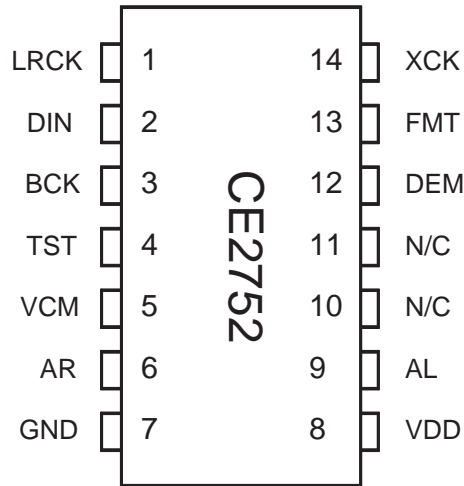
Block Diagram:



DV-SL800W

IC401B, STEREO AUDIO DAC, 24-bit, 192kHz

Pin Assignment:



Pin Description:

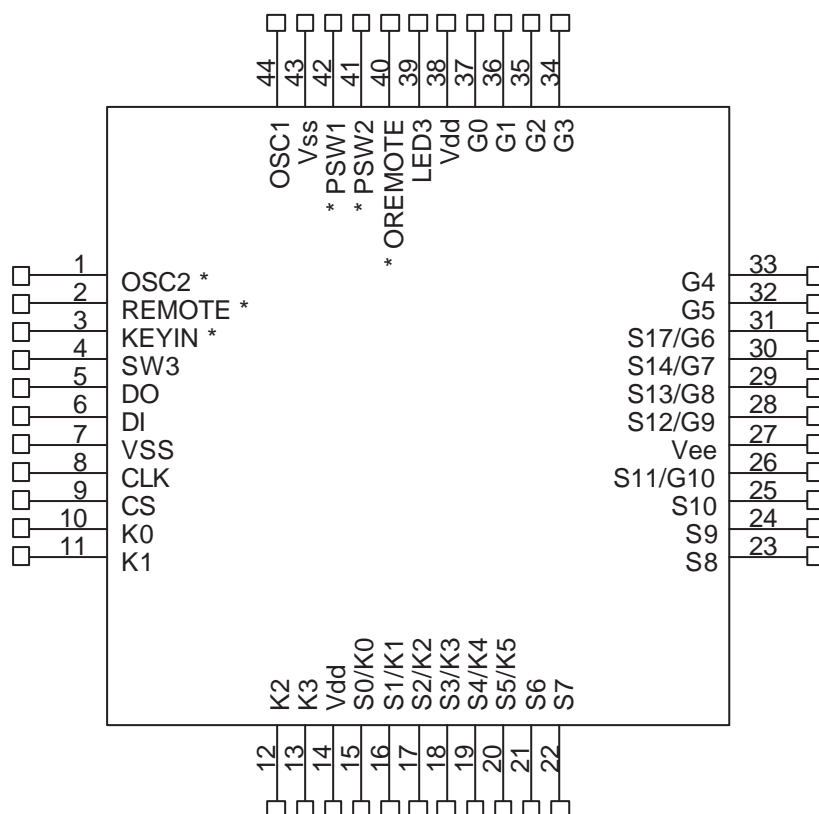
Pin Name	Pin #	Type	Description
LRCK	1	I	Left/Right Channel Clock pin. For Left justified mode, a high in SF indicates Left Channel Data, a low in SF indicates Right Channel Data. For I2S mode, a low in SF indicates Left Channel Data, a high in SF indicates Right Channel Data.
DIN	2	I	Serial Audio Data Input.
BCK	3	I	Audio Serial Data Clock Input.
TST	4	I	Test pin. This pin should be connected to ground.
VCM	5	I/O	Common voltage De-coupling Pin Should be Connected to a 22 uF capacitor in parallel with a 0.1 uF.
AR	6	O	Analog right channel output
GND	7	GND	Ground
DVDD	8	+3.3V	3.3 or 5 volt power supply.
AL	9	O	Analog left channel output
N/C	10,11	N/C	Not used, can connected to ground.
DEM	12	I	'low' in normal operation, 'high' to enable de-emphasis filter.
FMT	13	I	'low' if the input is left justified format. 'high' if the input is I ² S format.
XCK	14	I	Master clock input.

IC2, VFD CONTROLLER/DRIVER

Pin Description:

Pin Number	Name	I/O	Definitions
1	OSC2	O	Crystal Oscillator output pin.
44	OSC1	I	Crystal Oscillator input pin, provides oscillation frequency for IC.
2	REMOTE	I	Remote control signal receiver pin.
3	KEYIN	I	External key-in signal receiver pin.
4	SW3	I	Multi-purpose input pin.
5	DO	O	Serial data output pin. When the shift clock falling edge, the serial data outputting from the low order bit. This is an NMOS open-drain output pin.
6	DI	I	Serial data input pin. When the shift clock rising edge, the serial data inputting from the low order bit.
7, 43	Vss	-	Power supply ground.
8	CLK	I	Clock signal. To read data at the rising edge, and outputs data at the falling edge.
9	$\overline{\text{CS}}$	I	Initializes serial interface at the rising or falling edge, to set the VDTR6312 to waiting for receive command. After the CS fallen, the input data process become a command. After command processed, terminate the current process, and initialized the serial interface. If CS is high voltage, CLK signal will be in vain.
10~13	K0~K3	I	Keying data input pins.
14, 38	VDD	-	Positive power supply.
15~20	S0/K0~S5/K5	O	Composite output pins of segment output signal and key scanning signal.
21~25	S6~S10	O	Segment output pins, PMOS open-drain with pull-low resistor output.
26, 28~31	S11/G10~S15/G6	O	Segment or Grid driver output pins. These pins are selectable for segment or grid driving, and PMOS open-drain with pull-low resistor output.
27	Vee	-	VFD power supply pin.
37~32	G0~G5	O	Grid driver output pins, PMOS open-drain with pull-low resistor output.
39	LED3	O	LED CMOS driver output pins, and maximum output current up to 20mA.
40	OREMOTE	O	Remote control signal output pin.
41~42	PSW1~PSW2	O	External device power control pins.

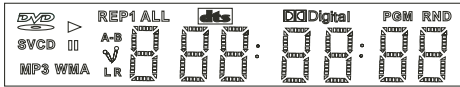
Pin Configuration:



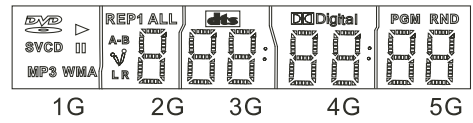
FL DISPLAY

92LKL00003810

PATTERN



GRID ASSIGNMENT

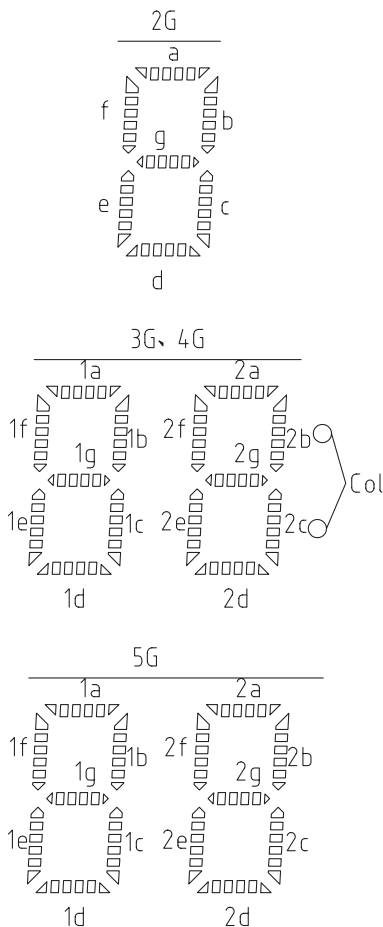


PIN CONNECTION

PIN NO.	1	2	3	4	5	6	7	8	9
CONNECTION	F1	F1	NP	P1	P2	P3	P4	P5	P6
PIN NO.	10	11	12	13	14	15	16	17	18
CONNECTION	P7	P8	P9	P10	P11	P12	P13	P14	P15
PIN NO.	19	20~24	25	26	27	28	29	30	31
CONNECTION	P16	NC	1G	2G	3G	4G	5G	NP	F2
PIN NO.	32								
CONNECTION	F2								

NOTE: F: FILAMENT
 G: GRID
 NC: NO CONNECTION
 NP: NO PIN
 P: ANODE

PATTERN DETAIL



ANODE CONNECTION

	1G	2G	3G	4G	5G
P1	/	d	2d	2d	2d
P2	/	e	2e	2e	2e
P3	/	c	2c	2c	2c
P4	/	g	2g	2g	2g
P5	/	f	2f	2f	2f
P6	/	b	2b	2b	2b
P7	/	a	2a	2a	2a
P8	/	/	Col	Col	RND
P9		R	1d	1d	1d
P10	▷	L	1e	1e	1e
P11	WMA	Ⓜ	1c	1c	1c
P12	MP3	-B	1g	1g	1g
P13	CD	A	1f	1f	1f
P14	V	ALL	1b	1b	1b
P15	S	1	1a	1a	1a
P16	DVD	REP	dts	Digital	PGM

SHARP PARTS GUIDE

DVD PLAYER

MODEL DV-SL800W

CONTENTS

- | | |
|-------------------------|--|
| [1] INTEGRATED CIRCUITS | [8] ARRAY PARTS |
| [2] TRANSISTORS | [9] CAPACITORS |
| [3] DIODES | [10] RESISTORS |
| [4] FILTER | [11] OTHER CIRCUITRY PARTS |
| [5] VIBRATORS/CRYSTALS | [12] P.W.B. ASSEMBLY (Non Replacement Items) |
| [6] TRANSFORMER | [13] CABINET PARTS (MAIN UNIT) |
| [7] COILS | [14] ACCESSORIES/PACKING PARTS |

Parts marked with "△" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
[1] INTEGRATED CIRCUITS					
IC1	92LRCI00455806	AG			GP IC 8P AZ4558AM-E1 SOIC-8 AAC DUAL LOW NOISE OPER. AMP
IC2	92LRCI00631205	AN			GP IC 44P V6312A QFP VAITECH VFD CONTROLLER / DRIVER
IC101	92LRCI00820204	BM			IC 216PIN SPHE82025 LQFP SUNPLUS DVD SINGLE CHIP MPEG A / V PROCESSOR
IC104	92LRCI24000205	AN			IC 8P AF24LLC02A SOP CERAMATE 2K.BIT SERIAL EEPROM
IC105	92LRCI00586901	AP			IC 28PIN AM5869S HSOP AMTEK 5-CH BTL LF DRIVER FOR DVD PLAYER
IC106,IC107	92LRCI16161001	AW			IC 50PIN HY57V161610ET-7 TSOPII 143MHZ 2BANKSX512KX16BIT
IC120	92LRCI00080903	AK			GP IC 3PIN STM809SEURF SOT23-3 RESET 2.93V MICROCONT PWR SUPPLY
IC402	92LRCI00455806	AG			GP IC 8P AZ4558AM-E1 SOIC-8 AAC DUAL LOW NOISE OPER. AMP
IC103A	92LRCI29004000	AV			IC 32 PIN MX29LV040CTC-70G TSOP MXIC CMOS 3V 4M FLASH MEMORY
IC401B	92LRC00275202	AM			GP IC 14 PIN CE2752C SOIC CEI 24 BIT 192KHz
PC1	92LRHO00081702	AG			GP OPTICAL SENSOR 4P CTR:200-400 EVERLIGHT:EL-817 (C)
U1	92LRHI00431001	AE			GP IC 3PIN TL431 TO-92 CHANG JIANG VOLTAGE REGULATOR
[2] TRANSISTORS					
Q1	92LRHM00406001	AL			MOSFET SSS4N60B TO-220F N-CH FAIRCHILD 4A 600V (POWER PCB)
Q1	92LRCN00387501	AE			GP XISTR NPN KTC3875-Y SOT23 CHANGJIANG HFE:120-240 (KARAOKE PCB)
Q2	92LRCP00390601	AD			XISTR NPN PMBT3904 SOT23 PHILIPS (POWER PCB)
Q2	92LRCN00387501	AE			GP XISTR NPN KTC3875-Y SOT23 CHANGJIANG HFE:120-240 (KARAOKE PCB)
Q3	92LRAN20181501	AC			GP XISTR NPN 2SC1815-GR TOSHIBA
Q4	92LRAS00016901	AE			GP TRIACS 3P BT169D SOT54 (TO92) 0.5A THYRISTORS LOGIC LEVEL
Q5	92LRCN00390405	AC			XISTR NPN PMBT3904 SOT23 PHILIPS NPN SWITCHING TRANSISTOR
Q6	92LRAN20181501	AC			GP XISTR NPN 2SC1815-GR TOSHIBA
Q7	92LRAP00101501	AC			GP XISTR PNP A1015 Y TO-92 J.CHANGJIANG
Q101,Q102	92LRCP20113204	AE			GP XISTR PNP 2SB1132R SOT-89 GR HFE:180-390
Q103,Q104	92LRCM20301802	AC			GP MOSFET 2SK3018 30V/0.1A SOT23 GR N-CH
Q105	92LRCN00390405	AC			XISTR NPN PMBT3904 SOT23 PHILIPS NPN SWITCHING TRANSISTOR
Q305	92LRCN00390405	AC			XISTR NPN PMBT3904 SOT23 PHILIPS NPN SWITCHING TRANSISTOR
Q401	92LRCN00390405	AC			XISTR NPN PMBT3904 SOT23 PHILIPS NPN SWITCHING TRANSISTOR
Q402	92LRCN00390405	AC			XISTR NPN PMBT3904 SOT23 PHILIPS NPN SWITCHING TRANSISTOR
Q403~Q407	92LRCP00390601	AD			GP XISTR PNP SST3906 SOT ROHM GENERAL PURPOSE
Q901, Q902	92LRAP00855001	AC			XISTR PNP 8550SS-D TO-92 CJ GP HFE:160-300 1W OUTPUT AM
[3] DIODES					
D1	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123 (KARAOKE PCB)
D1	92LRAD11400710	AC			GP DIODE 1N4007 AI (POWER PCB)
D2	92LRAD11400710	AC			GP DIODE 1N4007 AI (POWER PCB)
D2	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123 (KARAOKE PCB)
D3	92LRAD11400710	AC			GP DIODE 1N4007 AI
D4	92LRAD11400710	AC			GP DIODE 1N4007 AI
D5	92LRAD10010710	AC			GP DIODE FR107 1A 1000V
D7	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123
D10	92LRAD10010710	AC			GP DIODE FR107 1A 1000V
D12,D13	92LRAD10010710	AC			GP DIODE FR107 1A 1000V
D14	92LRHD11582211	AF			GP RECTIFIER IN5822 3A 45V W/KINK SCHOTTKY BARRIER
D101,D102	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123 (CONTROL PCB)
D101,D102	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123 (MAIN PCB)
D103~D105	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123
D203,D204	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123
D210	92LKED20000310	AC			GP LED 3 DIA RED ROUND
D301~ D304	92LRAD11400710	AC			GP DIODE 1N4007 AI
D305, D306	92LRAD10010710	AC			GP DIODE FR107 1A 1000V
D308	92LRAD10010410	AC			GP DIODE HER104 1A 300V 50mS AI
D311	92LRHD11582211	AF			GP RECTIFIER IN5822 3A 45V W / KINK SCHOTTKY BARRIER
D404	92LRCD11414811	AB			GP DIODE CHIP BAV16W / IN4148 (SKYWELL) SOT-123
D902	92LRAD1140011A	AB			DIODE RECTIFIER IN4001 1A 35VRMS
ZD1,ZD3	92LRCZ00501810	AC			CHIP ZENER 18V 5% 0.5W (J3) MOTOROLA MMSZ5248BTP1
ZD2	92LRCZ00500530	AC			CHIP ZENER 5.1V 5% 0.5W (E1) SOD-123 MMSZ5231B
ZD4	92LRAZ01000620	AC			GP DIODE ZNR 6.2V 5% 1W DO-41 IN4735A
ZD301~ZD308	92LRCZ00500710	AC			GP CHIP ZENER 6.8V 5% 0.5W (E5) SOD-123 MOTOROLA MMSZ5235BT1
[4] FILTER					
△ LF1	92LJFT00100701	AK			LINE FILTER 20mH ET-20 EF001
[5] VIBRATORS/CRYSTALS					
XT1	92LJQC15810060	AG			GP CRYSTAL 27MHz HC49 / US + / -15ppm DONGYUAN SHORT DP3080
[6] TRANSFORMER					
△ T1	92L TSA10000815	AE			SW TRANSFORMER EEL-22 15W OUT / 5 ET001
[7] COILS					
FB101	92LSCB00603100				FERRITE 60 OHM 100MHz +/-25% 0603 SMT TYPE
FB123	92LSCB00603060	AB			FERRITE 600 OHM 0603 SMT TYPE 20%
FB125~FB137	92LSCB00603060	AB			FERRITE 600 OHM 0603 SMT TYPE 20%
FB301~FB307	92LSCB00603010	AC			GP CHIP BEAD 100 OHM AT 100MHz SMD 0603 GTH DP301
FB309	92LSCB00603010	AC			GP CHIP BEAD 100 OHM AT 100MHz SMD 0603 GTH DP301
FB401,FB402	92LSCB00603060	AB			FERRITE 600 OHM 0603 SMT TYPE 20%
FB901	92LSCB00603112	AC			GP CHIP BEAD 600 OHM 25% AT 100MHz 2A 0603 MICROGATE:MGLB1608-600T-L
FB902	92LSCB00603060	AB			FERRITE 600 OHM 0603 SMT TYPE 20%
FB904,FB905	92LSCB00603060	AB			FERRITE 600 OHM 0603 SMT TYPE 20%
FB907,FB910	92LSCB00603060	AB			FERRITE 600 OHM 0603 SMT TYPE 20%
FB912,FB913	92LSCB00603110	AB			GP CHIP BEAD 600 OHM 25% AT 100MHz IDC:200 EROCORE:CB160808T-601Y
FB918,FB919	92LSCB00603110	AB			GP CHIP BEAD 600 OHM 25% AT 100MHz IDC:200 EROCORE:CB160808T-601Y

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
[7] COILS					
FB912,FB913	92LSCB00603110	AB			GP CHIP BEAD 600 OHM 25% AT 100MHz IDC:200 EROCORE:CB160808T-601Y
FB918,FB919	92LSCB00603110	AB			GP CHIP BEAD 600 OHM 25% AT 100MHz IDC:200 EROCORE:CB160808T-601Y
L2	92LSIN00360000	AD			GP INDUC 20uH 10% D0.45x27.5Ts
L11,L12	92LSCN02360000	AC			GP CHIP INDUC 10uH 10% SMD 0805 SGM12012K100KT
L301~L304	92LSCN02350090	AC			GP INDUCTOR 2.4uH 5% SMD 0805 VIDEO SW
L310	92LSCN12260090	AC			GP CHIP INDUC 1.8uH 10% SMD 0603 IDC:200 EROCORE:CB160808T-601Y
R10,R11	92LSCN02260100				INDUCTOR 101CH 10% Q=35 0603 SMT GP MGFI 1608 D00 KT-LF
[8] ARRAY PARTS					
RB101, RB102	92LQCP01508133	AC			GP CHIP ARRAY 4x33 OHM 1 / 10 W 5% 8 PIN CHIP
RB105~RB107	92LQCP01508133	AC			GP CHIP ARRAY 4x33 OHM 1 / 10 W 5% 8 PIN CHIP
RB110~RB111	92LQCP01508133	AC			GP CHIP ARRAY 4x33 OHM 1 / 10 W 5% 8 PIN CHIP
RB113~RB117	92LQCP01508133	AC			GP CHIP ARRAY 4x33 OHM 1 / 10 W 5% 8 PIN CHIP
[9] CAPACITORS					
C1	92LPLE0995K200	AG			GP COND ELECT 15 uF 400V 20% 105°C SIZE=D10 X H21 X P5 MM (POWER PCB)
C1~C5	92LPRE03954090	AC			GP COND ELECT 4.7 uF 16V 20% 85°C (KARAOKE PCB)
C2	92LPVD2354Q020	AD			GP COND DISC 4700 pF 1KV 10% Y5P (POWER PCB)
C3	92LPYL43957047	AC			GP CHIP CAP 0.47 uF 50V 20% 0805 Y5V (POWER PCB)
C4	92LPRM0373A020	AC			GP COND MYLAR 0.001 uF 100V 5% AI (POWER PCB)
C5	92LPYL45647020	AB			GP CHIP CAP 0.0047 uF 50V 10% 0805 TYPE X7R
C6	92LPYL45647030	AC			GP CHIP CAP 0.01 uF 50V 10% 0805 TYPE Y5V (POWER PCB)
C6	92LPRE03954010	AC			GP COND ELECT 100 uF 16V 20% 85°C (KARAOKE PCB)
C7	92LPRE03954021	AC			GP COND ELECT 10 uF 16V 20% 85°C (KARAOKE PCB)
C7	92LPRE03954022	AC			GP COND ELECT 220 uF 16V 20% 85°C (POWER PCB)
C8	92LPRE99954047	AH			GP COND ELECT 47 uF 16V 20% 105°C MINI SIZE DTA150 / SANYO (POWER PCB)
C8,C9	92LPXL45647071	AA			GP COND ELECT 470 uF 50V 10% 0603 TYPE X7R (KARAOKE PCB)
C9	92LPRE03956011	AC			GP COND ELECT 100 uF 35V 20% 85°C (POWER PCB)
C10	92LPXL4564701A	AA			GP CHIP CAP 220 pF 50V 10% 0603 TYPE X7R
C11	92LPXL4564701A	AA			GP CHIP CAP 220 pF 50V 10% 0603 TYPE X7R (KARAOKE PCB)
C11	92LPVE29954010	AD			GP COND ELECT 330 uF 16V 20% 105°C LOW ESR D8 X L12MM (POWER PCB)
C12	92LPRE03954022	AC			GP COND ELECT 220 uF 16V 20% 85°C
C13	92LPVE03953020	AF			GP COND ELECT 2200 uF 10V 20% 85°C CUT 3.5MM (USE IN POWER PCB)
C13	92LPXL45647040	AC			GP COND ELECT 0.1 uF 50V 10% 0603 TYPE X7R (USE IN KARAOKE PCB)
C14	92LPRE03953047	AC			GP COND ELECT 470 uF 10V 20% 85°C (USE IN POWER PCB)
C14,C16	92LPXL43954050	AB			GP COND ELECT 0.1 uF 16V 20% 0603 TYPE Y5V (USE IN KARAOKE PCB)
C15	92LPXL43954050	AB			GP COND ELECT 0.1 uF 16V 20% 0603 TYPE Y5V
C16	92LPYL43967050	AC			GP CHIP CAP 1 uF 50V +80-20% 0805 TYPE Y5V (USE IN POWER PCB)
C17,C18	92LPXL45647010	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C19	92LPVM0373A020	AC			GP COND MYLAR 0.0022 uF 100V 5%
C20	92LPRE03954010	AC			GP COND ELECT 100 uF 16V 20% 85°C
C21	92LPXL45647040	AC			GP COND ELECT 0.1 uF 50V 10% 0603 TYPE X7R
C101~C137	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C138	92LPXL45647010	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C140,C141	92LPXL41037001	AB			GP CHIP CAP 10 pF 50V 5% 0603 TYPE NPO
C142	92LPXL45647010	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C143	92LPXL41037001	AB			GP CHIP CAP 10 pF 50V 5% 0603 TYPE NPO
C144,C145	92LPXL45647010	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C152	92LPME03954010	AC			GP COND ELECT 100 uF 16V 20% Size=5x11mm AI 85C P=2.5mm
C153	92LPME03954000	AC			GP COND ELECT 10 uF 16V 20% 85C P=2.5mm AI
C154~C158	92LPXL45647081	AA			GP CHIP CAP 680 pF 50V 10% 0603 TYPE X7R
C159~C162	92LPXL45647030	AB			GP CHIP CAP 0.01 uF 50V 10% 0603 TYPE X7R
C163~C166	92LPXL43954050	AB			GP CHIP CAP 1 uF 16V 20% TYPE Y5V
C167	92LPXL45647083	AB			GP CHIP CAP 0.068 uF 50V 10% 0603 TYPE X7R
C168	92LPXL45647010	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C169,C170	92LPXL41037047	AB			GP CHIP CAP 47 pF 50V 5% 0603 TYPE NPO
C173,C174	92LPME03954000	AC			GP COND ELECT 10 uF 16V 20% 85°C P=2.5mm AI
C176	92LPME83954010	AC			GP COND ELECT 100 uF 16V 20% AI H=5mm P=2.5mm
C177~C179	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C180,C181	92LPME03954047	AC			GP COND ELECT 47 uF 16V 20% SIZE=5x11mm AI 85C P=2.5mm
C182,C183	92LPME89954000	AC			GP COND ELECT 47 uF 16V 20% 105C AI Type D=5mm H<=5mm P=2.5mm DP3
C184	92LPXL45647031	AA			GP CHIP CAP 300 pF 50V ±10% 0603 TYPE X7R
C186	92LPXL45647047	AC			GP CHIP CAP 0.047 uF 50V 10% 0603 TYPE X7R
C187	92LPXL45647021	AA			GP CHIP CAP 820 pF 50V 10% 0603 TYPE X7R
C188	92LPXL45645040	AC			GP CHIP CAP 0.22 uF 25V 10% 0603 TYPE X7R
C191	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C194,C195	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C196,C198	92LPME03954010	AC			GP COND ELECT 100 uF 16V 20% Size=5x11mm AI 85C P=2.5mm
C199,C200	92LPXL41037000	AA			GP CHIP CAP 33 pF 50V 5% 0603 TYPE NPO
C201~C203	92LPXL41037000	AA			GP CHIP CAP 33 pF 50V 5% 0603 TYPE NPO (MAIN PCB)
C201~C203	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C204,C205	92LPXL41037000	AA			GP CHIP CAP 33 pF 50V 5% 0603 TYPE NPO
C206	92LPME83954010	AC			GP COND ELECT 100 uF 16V 20% AI H=5MM P=2.5mm (KEY PCB)
C206,C207	92LPXL41037000	AA			GP CHIP CAP 33 pF 50V 5% 0603 TYPE NPO (MAIN PCB)
C207	92LPME83954010	AC			GP COND ELECT 100 uF 16V 20% AI H=5MM P=2.5mm (KEY PCB)
C208,C209	92LPXL41037000	AA			GP CHIP CAP 33 pF 50V 5% 0603 TYPE NPO
C210	92LPXL45647020	AC			GP CHIP CAP 0.001 uF 50V 10% 0603 TYPE X7R
C211,C212	92LPXL45647020	AA			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C213	92LPXL45647033	AA			GP CHIP CAP 330 pF 50V 10% 0603 TYPE X7R
C214,C215	92LPXL45647072	AA			GP CHIP CAP 0.0047 uF 50V 10% 0603 TYPE X7R
C216	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C217,C218	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C219	92LPXL45647030	AB			GP CHIP CAP 0.01 uF 50V 10% 0603 TYPE X7R
C221~C239	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
[9] CAPACITORS					
C301~C308	92LPXL45647010	AA			GP CHIP CAP 470 pF 50V 10% 0603 TYPE X7R (USE IN MAIN PCB)
C309	92LPXL41037050	AA			GP CHIP CAP 15 pF 50V 5% 0603 TYPE NPO
C310,C311	92LPXL41037050	AA			GP CHIP CAP 15 pF 50V 5% 0603 TYPE NPO (USE IN MAIN PCB)
C312~C315	92LPXL41037050	AA			GP CHIP CAP 15 pF 50V 5% 0603 TYPE NPO
C316	92LPXL41037050	AA			GP CHIP CAP 15 pF 50V 5% 0603 TYPE NPO (USE IN MAIN PCB)
C401~C403	92LPME03954000	AC			GP COND ELECT 10 uF 16V 20% 85°C P=2.5mm AI
C404	92LPME03954010	AC			GP COND ELECT 100 uF 16V 20% Size=5x11mm AI 85C P=2.5mm
C405	92LPME03954000	AC			GP COND ELECT 10 uF 16V 20% 85°C P=2.5mm AI
C408,C409	92LPXL45647018	AA			GP CHIP CAP 180 pF 50V 10% 0603 TYPE X7R
C410,C411	92LPXL45647020	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C412~C414	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C416	92LPME03954010	AC			GP COND ELECT 100 uF 16V 20% Size=5x11mm AI 85C P=2.5mm
C421,C427	92LPME03954022	AC			GP COND ELECT 220 uF 16V 20% 85°C
C422~C425	92LPXL45647056	AA			GP CHIP CAP 0.0056 uF 50V 10% 0603 TYPE X7R
C426	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C427	92LPME03954022	AC			GP COND ELECT 220 uF 16V 20% 85°C
C430~C432	92LPXL45647010	AA			GP CHIP CAP 100 pF 50V 10% 0603 TYPE X7R
C901	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C904,C905	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C907,C908	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C911~C913	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C916,C919	92LPME03954010	AC			GP COND ELECT 100 uF 16V 20% Size=5x11mm AI 85°C P=2.5mm
C920~C932	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
C934	92LPME03954010	AC			GP COND ELECT 100 uF 16V 20% Size=5x11mm AI 85°C P=2.5mm
C936,C941	92LPME03953010	AC			GP COND ELECT 100 uF 10V 20% AI 85°C P=2.5mm Size=5x11mm
C938	92LPME03954022	AC			GP COND ELECT 220 uF 16V 20% 85°C
C939,C940	92LPXL45647040	AC			GP CHIP CAP 0.1 uF 50V 10% 0603 TYPE X7R
CX1	92LPVX2024F042	AE			GP COND SAFETY 0.1 uF 250V +/-10% X2 P=15MM CUT 3.5MM
CY3	92LPVY1705F120	AF			GP COND SAFETY 0.0033 uF Y1 250V 20% X1 400V WD16E332MACT4KV (PAN)
[10] RESISTORS					
R1,R2	92LQCF0150308C	AA			GP CHIP RES. 82K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R1,R2	92LQCF04501040	AA			GP CHIP RES. 470K OHM 1 / 4W 5% CF 1206 SMT TYPE (POWER PCB)
R3	92LQHF10500040	AC			GP RES.100K OHM 1W 5% 0805 SMT TYPE (POWER PCB)
R3	92LQCF01503073	AA			GP CHIP RES. 47K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R4	92LQCF0450109A	AA			GP CHIP RES. 4.7 OHM 1 / 4W 5% 1206 SMT TYPE (POWER PCB)
R4,R5	92LQCF01503040	AA			GP CHIP RES. 100K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R5	992LQCF04500024	AA			GP CHIP RES. 820K OHM 1 / 4W 5% CF (POWER PCB)
R6	92LQCF04501082	AA			GP CHIP RES. 820K OHM 1 / 4W 5% 1206 SMT TYPE
R6~R8	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R7	92LQCF04501093	AA			GP CHIP RES. 39K OHM 1 / 4W 5% CF 1206 SMT TYPE (POWER PCB)
R8	92LQCF0450156A	AA			GP CHIP RES. 560 OHM 1 / 4W 5% 1206 SMT TYPE
R9	92LQCF0850202A	AA			GP CHIP RES. 1K OHM 1 / 8W 5% 0805 SMT TYPE (POWER PCB)
R9	92LQCF01503030	AA			GP CHIP RES. 30K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R10	92LQCF04501010	AA			GP CHIP RES. 470 OHM 1 / 4W 5% CF 1206 SMT TYPE
R11	92LQCF08502022	AA			GP CHIP RES. 220 OHM 1 / 8W 5% 0805 SMT TYPE
R12	92LQCF0150303B	AA			GP CHIP RES. 36K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R12	92LQCF08502030	AA			GP CHIP RES. 10K OHM 1 / 8W 5% 0805 SMT TYPE
R13	92LQCF0450102A	AA			GP CHIP RES. 4.7K OHM 1 / 4W 5% CF 1206 SMT TYPE (POWER PCB)
R13,R14	92LQCF01503073	AA			GP CHIP RES. 47K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R14	92LQCF0450109A	AA			GP CHIP RES. 4.7 OHM 1 / 4W 5% 1206 SMT TYPE
R15	92LQCF01503022	AA			GP CHIP RES. 220 OHM 1 / 10W 5% 0603 SMT TYPE
R16	92LQCF01503030	AA			GP CHIP RES. 30K OHM 1 / 10W 5% TF 0603 SMT TYPE (KARAOKE PCB)
R16,R17	92LQCF0450109A	AA			GP CHIP RES. 4.7 OHM 1 / 4W 5% 1206 SMT TYPE
R17	92LQCF0150302A	AA			GP CHIP RES. 2K OHM 1 / 10W 5% 0603 SMT TYPE (KARAOKE PCB)
R18	92LQCF0150302Z	AA			GP CHIP RES. 2.2K OHM 1 / 10W 5% 0603 SMT TYPE
R19	92LQCF01503010	AA			GP CHIP RES. 100 OHM 1 / 10W 5% 0603 SMT TYPE
R20	92LQCF01503021	AA			GP CHIP RES. 200 OHM 1 / 10W 5% 0603 SMT TYPE
R21	92LQCF04501030	AA			GP CHIP RES. 10K OHM 1 / 4W 5% CF 1206 SMT TYPE
R21	92LQCF01503000	AA			GP CHIP RES. 0 OHM 1 / 10W 5% TF 0603 SMT TYPE
R22	92LQCF0450100A	AA			GP CHIP RES. 0 OHM JUMPER WIRE 5% 1206 SMT TYPE
R23	92LQCF08502030	AA			GP CHIP RES. 10K OHM 1 / 8W 5% 0805 SMT TYPE
R25	92LQCF0450175A	AA			GP CHIP RES. 750 OHM 1 / 4W 5% 1206 SMT TYPE
R27	92LQCF045010AA	AA			GP CHIP RES. 10 OHM 1 / 4W 5% CF 1206 SMT TYPE
R28,R29	92LQCF04501310	AA			GP CHIP RES. 300 OHM 1 / 4W 5% CF 1206 SMT TYPE
R30	92LQCF08502068	AA			GP CHIP RES. 680 OHM 1 / 8W 5% 0805 SMT TYPE
R31	92LQCF0850202A	AA			GP CHIP RES. 1K OHM 1 / 8W 5% 0805 SMT TYPE
R32,R34	92LQCF08502030	AA			GP CHIP RES. 10K OHM 1 / 8W 5% 0805 SMT TYPE
R33	92LQCF08102072	AA			GP CHIP RES. 10.7K OHM 1 / 8W 1% 0805 SMT TYPE
R36	92LQCF08502050	AA			GP CHIP RES. 1M OHM 1 / 8W 5% 0805 SMT TYPE
R38	92LQCF0850202A	AA			GP CHIP RES. 1K OHM 1 / 8W 5% 0805 SMT TYPE
R39,R40	92LQCF08502033	AA			GP CHIP RES. 330 OHM 1 / 8W 5% 0805 SMT TYPE
R101	92LQCF08502000	AA			GP CHIP RES. 0 OHM JUMP WIRE 0805 SMT TYPE (USE IN CONTROL PCB)
R101	92LQCF01503047	AA			GP CHIP RES. 4.7K OHM 1 / 10W 5% 0603 SMT TYPE (USE IN MAIN PCB)
R103	92LQCF015030Y0	AA			GP CHIP RES. 33 OHM 1 / 10W 5% 0603 SMT TYPE
R104	92LQCF01503047	AA			GP CHIP RES. 4.7K OHM 1 / 10W 5% 0603 SMT TYPE
R105	92LQCF01503070	AA			GP CHIP RES. 47 OHM 1 / 10W 5% 0603 SMT TYPE
R107,R108	92LQCF015030Y0	AA			GP CHIP RES. 33 OHM 1 / 10W 5% 0603 SMT TYPE
R109	92LQCF01503015	AA			GP CHIP RES. 1.5K OHM 1 / 10W 5% 0603 SMT TYPE
R110	92LQCF0150303A	AA			GP CHIP RES. 20K OHM 1 / 10W 5% 0603 SMT TYPE
R111	92LQCF01503073	AA			GP CHIP RES. 47K OHM 1 / 10W 5% 0603 SMT TYPE
R112,R113	92LQCF01503051	AA			GP CHIP RES. 5.1K OHM 1 / 10W 5% 0603 SMT TYPE
R114~R116	92LQCF01503054	AA			GP CHIP RES. 150K OHM 1 / 10W 5% 0603 SMT TYPE
R134	92LQCF01503047	AA			GP CHIP RES. 4.7K OHM 1 / 10W 5% 0603 SMT TYPE
R136	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% TF 0603 SMT TYPE

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
[10] RESISTORS					
R137	92LQCF01503036	AA			GP CHIP RES. 390 OHM 1 / 10W 5% 0603 SMT TYPE
R138,R139	92LQCF01503000	AA			GP CHIP RES. 0 OHM 1 / 10W 5% TF 0603 SMT TYPE
R140	92LQCF015030Y0	AA			GP CHIP RES. 33 OHM 1 / 10W 5% 0603 SMT TYPE
R141,R142	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% TF 0603 SMT TYPE
R143-R153	92LQCF01503000	AA			GP CHIP RES. 0 OHM 1 / 10W 5% TF 0603 SMT TYPE
R154,R155	92LQCF01503519	AA			GP CHIP RES. 5.1 OHM 1 / 10W 5% 0603 SMT TYPE
R156,R157	92LQCF01503040	AA			GP CHIP RES. 100K OHM 1 / 10W 5% 0603 SMT TYPE
R158,R159	92LQCF01503071	AA			GP CHIP RES. 470 OHM 1 / 10W 5% 0603 SMT TYPE
R160-R162	92LQCF01503074	AA			GP CHIP RES. 470K OHM 1 / 10W 5% 0603 SMT TYPE
R163	92LQCF01103002	AA			GP CHIP RES. 33K OHM 1 / 10W 1% 0603 SMT TYPE
R164	92LQCF01103001	AA			GP CHIP RES. 1.2K OHM 1 / 10W 1% 0603 SMT TYPE
R166,R167	92LQCF01503000	AA			GP CHIP RES. 0 OHM 1 / 10W 5% TF 0603 SMT TYPE
R170	92LQCF0150309A	AA			GP CHIP RES. 1 OHM 1 / 10W 5% 0603 SMT TYPE
R171-R174	92LQCF01503047	AA			GP CHIP RES. 4.7K OHM 1 / 10W 5% 0603 SMT TYPE
R175	92LQCF0150308A	AA			GP CHIP RES. 68K OHM 1 / 10W 5% 0603 SMT TYPE
R176,R177	92LQCF015030Z2	AA			GP CHIP RES. 2.2K OHM 1 / 10W 5% 0603 SMT TYPE
R178	92LQCF01503040	AA			GP CHIP RES. 100K OHM 1 / 10W 5% 0603 SMT TYPE
R184-R187	92LQCF015030Y0	AA			GP CHIP RES. 33 OHM 1 / 10W 5% 0603 SMT TYPE
R188	92LQCF01503047	AA			GP CHIP RES. 4.7K OHM 1 / 10W 5% 0603 SMT TYPE
R201	92LQCF08502033	AA			GP CHIP RES. 330 OHM 1 / 8W 5% 0805 SMT TYPE
R202	92LQCF08502018	AA			GP CHIP RES. 1.8K OHM 1 / 8W 5% 0805 SMT TYPE
R203-R207	92LQCF06500003	AA			GP CHIP RES. 10K OHM 1 / 6W 5% CF
R209,R210	92LQCF06500000	AA			GP CHIP RES. 10 OHM 1 / 6W 5% CF
R211	92LQCF01503056	AA			GP CHIP RES. 5.6K OHM 1 / 10W 5% 0603 SMT TYPE
R212,R213	92LQCF01503003	AA			GP CHIP RES. 10K OHM 1 / 10W 5% 0603 SMT TYPE
R214	92LQCF06500013	AA			GP CHIP RES. 51K OHM 1 / 6W 5% CF
R215	92LQCF06500061	AA			GP CHIP RES. 560 OHM 1 / 6W 5% CF
R301-R304	92LQCF015030Z7	AA			GP CHIP RES. 75 OHM 1 / 10W 5% 0805 SMT TYPE
R305,R306	92LQCF01503010	AA			GP CHIP RES. 100 OHM 1 / 10W 5% 0603 SMT TYPE
R307	92LQCF01503003	AA			GP CHIP RES. 10K OHM 1 / 10W 5% 0603 SMT TYPE
R308	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% 0603 SMT TYPE
R309	92LQCF01503021	AA			GP CHIP RES. 200 OHM 1 / 10W 5% 0603 SMT TYPE
R401,R402	92LQCF01503023	AA			GP CHIP RES. 15K OHM 1 / 10W 5% 0603 SMT TYPE
R403,R404	92LQCF01503042	AA			GP CHIP RES. 2.4K OHM 1 / 10W 5% 0603 SMT TYPE
R405,R406	92LQCF01503003	AA			GP CHIP RES. 10K OHM 1 / 10W 5% 0603 SMT TYPE
R407,R408	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% 0603 SMT TYPE
R410-R413	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% 0603 SMT TYPE
R416	92LQCF0150302A	AA			GP CHIP RES. 2K OHM 1 / 10W 5% 0603 SMT TYPE
R417-R421	92LQCF01503002	AA			GP CHIP RES. 1K OHM 1 / 10W 5% 0603 SMT TYPE
R423	92LQCF01503003	AA			GP CHIP RES. 10K OHM 1 / 10W 5% 0603 SMT TYPE
R428-R431	92LQCF01503032	AA			GP CHIP RES. 3K OHM 1 / 10W 5% 0603 SMT TYPE
R432	92LQCF01503068	AA			GP CHIP RES. 6.8K OHM 1 / 10W 5% 0603 SMT TYPE
R433	92LQCF01503073	AA			GP CHIP RES. 47K OHM 1 / 10W 5% 0603 SMT TYPE
R434	92LQCF01503001	AA			GP CHIP RES. 10 OHM 1 / 10W 5% 0603 SMT TYPE
R437,R438	92LQCF01503071	AA			GP CHIP RES. 470 OHM 1 / 10W 5% 0603 SMT TYPE
R439	92LQCF01503032	AA			GP CHIP RES. 3K OHM 1 / 10W 5% 0603 SMT TYPE
R901	92LQCF0150303A	AA			GP CHIP RES. 20K OHM 1 / 10W 5% 0603 SMT TYPE
R902	92LQCF01503023	AA			GP CHIP RES. 12K OHM 1 / 10W 5% 0603 SMT TYPE
R903	92LQCF01503003	AA			GP CHIP RES. 10K OHM 1 / 10W 5% 0603 SMT TYPE
R904	92LQCF01503047	AA			GP CHIP RES. 4.7K OHM 1 / 10W 5% 0603 SMT TYPE
R905	92LQCF08502090	AA			GP CHIP RES. 2.2 OHM 1 / 8W 5% 0805 SMT TYPE
R906	92LQCF01503229	AA			GP CHIP RES. 2.2 OHM 1 / 10W 5% 0603 SMT TYPE
R907	92LQAF02500090	AA			GP CHIP RES. 3.3 OHM 1 / 2W 5% CF
R908	92LQCF01503001	AA			GP CHIP RES. 10 OHM 1 / 10W 5% 0603 SMT TYPE
[11] OTHER CIRCUITRY PARTS					
△ AC CORD	92LVPE00327911	AS			GP P. CORD 2P 1726 BK EUR (TIE X STEEL) 100W KE-21 B=3.96VH 00204921BW COR 0.5mm
△ AC CORD	92LVPE41A25310	BC			GPL. CORD 3PIN 1750mm BLK BS FUSE 3A 250V W/PVC BUSH, VOLEX PLUG:MP5
CON1	92LCCN39602Z14	AD			GP CONNECTOR 4P PITCH=3.96mm REMOVE PIN 2 & 3 H TYPE
CON2	92LCCN20000007	AC			GP CONNECTOR 7P PITCH=2.0mm B7B-PH-K TOP BASE
CON / WIRE	92LVFC24011040	AG			GP FFC CABLE 24P 240mm 20696 PITCH=0.5mm DR620
CON / WIRE	92LVFL40124400	AH			GP CON / WIRE 4P 150mm 2468#26 A .B=2mm GP RAINBOW DP3240
CON / WIRE	92LVFL50124400	AH			GP CON FLAT CABLE 5P 120mm 2468#26 RAINBOW A .B=2mm
CON / WIRE	92LVWA20000214	AH			GP CON / WIRE 6P 100mm 1007#28 A .B=2mm BLACK
CN1	92LVSW42445320	AL			GP CON / WIRE 4P 120mm 2547#28 GRAY A=2.0mm B=2012V
CN101	92LCHC05002024	AH			GP CHIP FFC CONN 24P P=0.5mm JS-1104B-2 CHYAO SHIUNN
CN102	92LCCN20000006	AC			GP CONNECTOR 6P PITCH=2.0mm B6B-PH-K TOP BASE
CN103	92LCCN20000005	AC			GP CONNECTOR 5P PITCH=2.0mm B5B-PH-K TOP BASE
CN105	92LCCN20000009	AD			GP CONNECTOR 9P PITCH=2.0mm B9B-PH-K TOP BASE
CN200	92LVFL90124600	AM			GP CON / WIRE 9P 150mm 2468#26 RAINBOW A=2.0MM B=2012H
CN401	92LCCN20000004	AC			GP CONNECTOR 4P PITCH=2.0mm B4B-PH-K TOP BASE
CN901	92LCCN20000007	AC			GP CONNECTOR 7P PITCH=2.0mm B7B-PH-K TOP BASE
D15	92LXJP22000003	AC			WIRE BARE 22 GA TINNED
△ F1	92LKHT02010030	AG			GP FUSE CERAMIC ICP 1A 250V TIME-LAG 4X10.5MM SMKO / VDE / CCC / UL
GND1	92LCSL20703500	AE			GP SOLDER LUG OD7.0xID3.5xT0.3mm NICKEL W / 5820-220AA
J2,J3	92LXJP22000003	AC			WIRE BARE 22 GA TINNED
JACK1,JACK2	92LJCM06430110	AG			GP PHONE JACK D6.43 3P YCG:CK-6.35-18H NI
JK101	92LJCR00630120	AK			GP RCA JACK 6P RD-BU-WT / GN-OR-RD RCA-613D-027 W / GND
JK102	92LJJC01000430	AK			GP RCA + DIN JK 1RCA + 4P DIN YEL W / GND RCA -125
JW1-JW6	92LXJP22000003	AC			WIRE BARE 22 GA TINNED
JW201-JW211	92LXJP22000003	AC			WIRE BARE 22 GA TINNED
K7-K9	92LMRW10600220	AC			GP TACT SW H 5MM 2P 160gF 15V 20MA 50MOHM RED EVQ11L05R
K10	92LMAW00600410	AC			GP TACT SW EVQ 227 0R5 H 5MM 2P 260gF 15V 20MA
K11,K12	92LMRW10600220	AC			GP TACT SW H 5MM 2P 160gF 15V 20MA 50MOHM RED EVQ11L05R

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
[11] OTHER CIRCUITRY PARTS					
RB201A TO RB201	92LVFL40125600	AK			GP C / WIRE 4P 130mm 2468#26 RAINBOW A=2012V B=2012H
RB208A TO RB208	92LVFL40126600	AG			GP C / WIRE 4P 180mm 2468#26 RAINBOW A, B=2012H DR31C0 / SCOTT
SN2	92LRHO20380501	AL			IRT SENSOR IRM-2638AS5F4 EVERLIGHT W / METAL BRACKET (RECEIVER)
SW1	92LXJP22000003	AC			WIRE BARE 22 GA TINNED
T1	92LCSL207035Z1	AC			GP SOLDER LUG OD 7.0xID 3.5xT 0.3mm 60MM W / 1007#18 BLK STP
T2	92LCSL20703505	AD			GP SOLDER LUG OD 7.0xID 3.5xT 0.3mm 120MM W / 1007#18 BLK STP=4MM
VFD2	92LKL00003810	AV			VFD 48.5 X 9MM 20075-1B06 IRICO-AOTOM PA75 X 20.5 X LEAD 10.5MM
VR1,VR2	92LMVR00221031	AG			GP VR 50K 20% R0911NOAH1B503FG0029 B SIGNAL L=20MM RADIAL
[12] P.W.B. ASSEMBLY (Non Replacement Items)					
	92LAPE20271051	BX			MAIN PCB ASS'Y
	92LAPE20226051	BC			KARAOKE PCB ASS'Y
	92LAPE20248052	CA			KEY1+ KEY2 + KEY3 PCB ASS'Y
	92LAPE20235514	BH			GP POWER PCB ASS'Y
[13] CABINET PARTS					
1	92LBPK22807502	AH			FUNCTION KNOB
2	92LBPK20806701	AG			VOLUME KNOB
3	92LGSE20017301	AD			BRACKET
4	92LBPK21807502	AH			OPEN KNOB
5	92LBPN20009102	AH			LENS
6	92LBPD20005301	AK			DVD DOOR
7	92LBPF20005501	AY			FRONT CAB
8	92LBPK20807502	AH			POWER KNOB
9	92LBPN20009001	AD			LED LENS
10	92LABN04R34301	BY			DVD MECHANISM ASSY
11	92LGSE10057801	BA			TOP COVER
12	92LGSE20017213	AQ			BACK PANEL
13	92LBRF40002601	AC			FOOT CUSHION
14	92LGSE20017101	AY			BOTTOM CHASSIS
15	92LDSS10002201	AC			SPACER
S1	92LHSF05308460	AB			M3.0xP0.5xL6
S2	92LHSP04030380	AA			T2.6xP0.91xL8
S3	92LHSP05005480	AB			T3.0xP1.06xL8
S4	92LHST4E308460	AB			M3.0xP0.5xL6
S5	92LHSW05308480	AB			M3.0xP0.5xL8
	92LYLB20800201	AC			CPA LABEL (SPORE SAFETY LABEL, PSM)
	92LYLB42000301	AF			POP LABEL
	92LYLB21100401	AC			SPEC LABEL
	92LYLB21100402	AD			SPEC LABEL (MADE IN MALAYSIA)
	92LYLB41110201	AC			SPEC LABEL (THAI)
	92LYLB42408101	AC			TISI LABEL (20mm X 20mm)
	92LYLB41110302	AC			HONG KONG LABEL (With Rating)
	92LYLB40804301	AF			SIRIM LABEL
[14] ACCESSORIES/PACKING PARTS					
	92LICC40012002	BA			Carton
	92LICG40000701	BB			Packing Case
	92LITF43108001	AG			Polyfoam Right
	92LITF43008001	AG			Polyfoam Left
	92LWIR24900102	BA			Remote Control
	92LFBY00141503	AH			Battery
	92LVRC30300114	AN			RCA Cable
	92LDHA40100101	AE			Handle
	92LYOM20005701	AP			Operation Manual
	92LYOM40013602	AN			Operation Manual (Hong Kong)
	92LYOM40013001	AN			Operation Manual (Thailand)
	92LCCP01000430	AF			Adaptor Plug (Philippines)
	92LIVA00000147	AC			Adaptor Plug Bag (L90 X W65 mm)
	92LYWC41004202	AD			G - Card (Hong Kong)
	92LYWC41004101	AD			G - Card (Philippines)
	92LYWC41004501	AF			G - Card (Indonesia)
	92LYLB20700103	AC			Bar Code Label (EAN : 4 9740 1999 0811)
	92LYLB12401814	AC			Contract Label (Colour - White Base)
	92LYLB42100501	AB			Production Date Label (43mm X 8mm)
	92LYLB40500201	AC			Serial No Label (55mm X 11mm)
	92LYLB12408801	AB			TISI Label (23mm X 23mm)
	92LYLB42409201	AB			Made in Malaysia Label (37mm X 6mm)
	92LICG40000701	BB			P-Case
	92LYLB42408501	AB			Hong Kong Safety Label (55mm X 15mm)
	92LYLB41602601	AB			G-Card Reminding Label (100mm X 50mm)
	92LYLB10900911	AC			Case Mark Label (35mm X 50mm)
	92LICC40012002	BA			Outer Carton (6 Sets Carton)
	92LYLB42408801	AB			Made in Malaysia Label (69mm X 10mm)
	92LYLB12101105	AB			Production Date Label (54mm X 10mm)

EXPLODED VIEW

MAIN UNIT

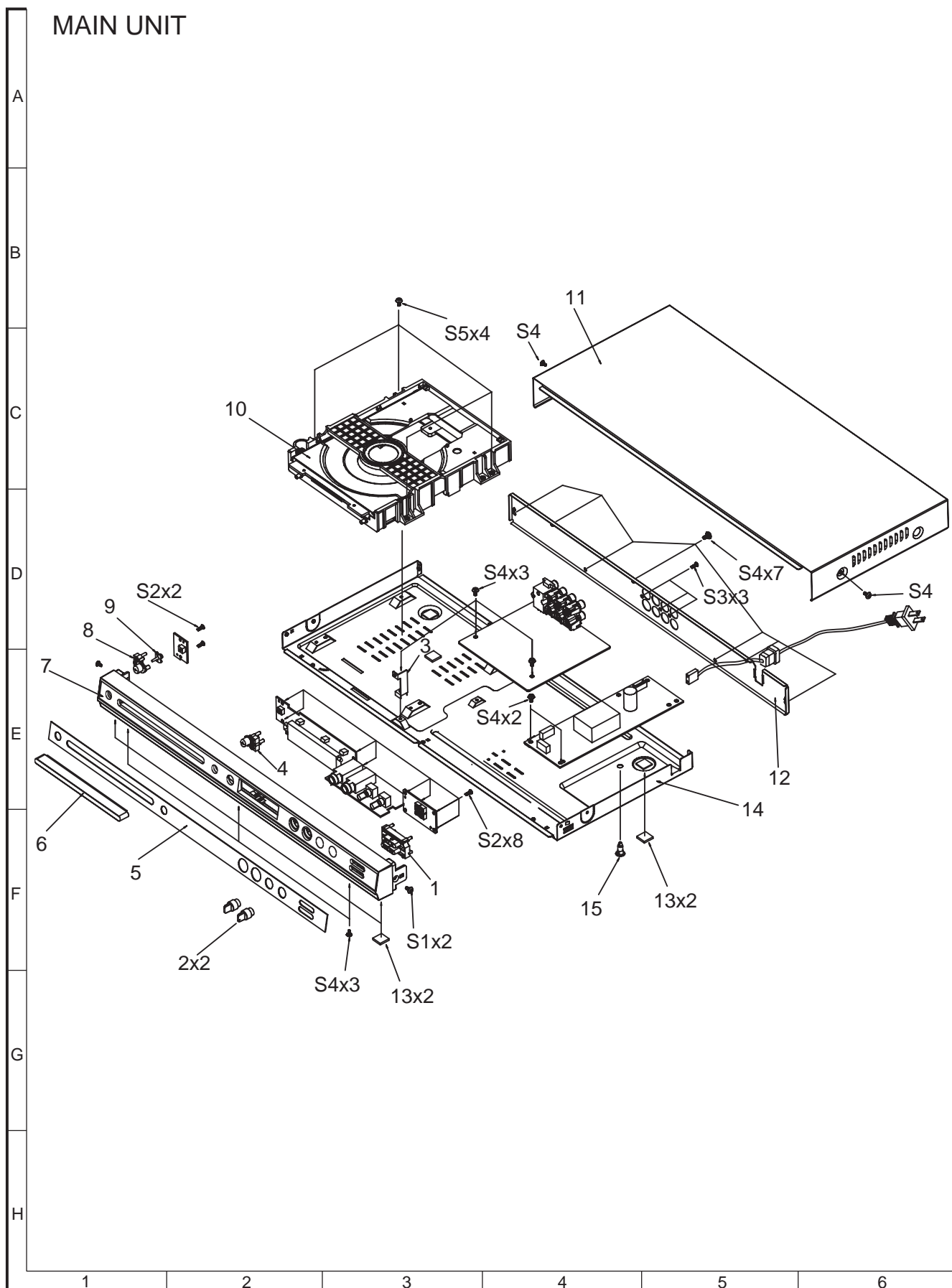


Figure 1: CABINET EXPLODED VIEW

DV-SL800W

-MEMO-

-MEMO-

SHARP

COPYRIGHT © 2005 BY SHARP CORPORATION

ALL RIGHTS RESERVED.

No Part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without prior written permission of the publisher.

SHARP CORPORATION
Sharp-Roxy Corporation
Sungai Petani, Kedah,
Malaysia

Printed in Malaysia

A0905-1MX•RR•M

EX